

Enhance Productivity in PCB Design with Online DFM Checks and Useful FloWare Modules

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Personal Introduction



Holger Schröter

Studies: Communications Engineering at TU Braunschweig

- Distance control radar at TU Braunschweig
- Development and project management for VCO and frequency synthesizer at Tyco Electronics
- Development of memory modules at Qimonda (Infineon)
- PCB Design Flow und Methodology at Infineon / Intel Mobile Phone
- Application Engineer at FlowCAD

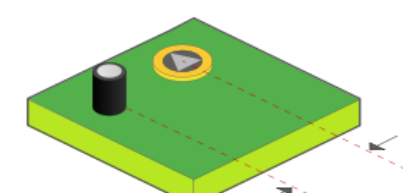
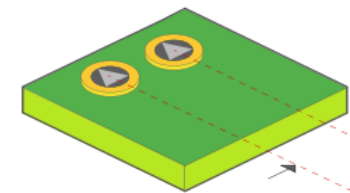
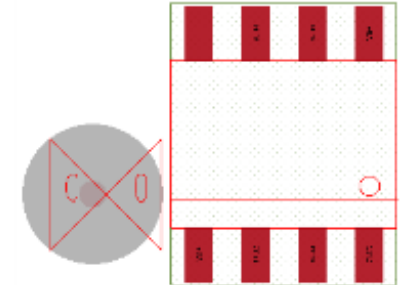
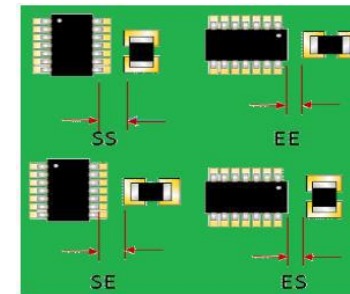
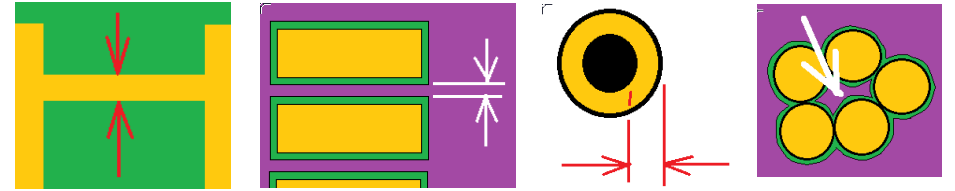
Overview

- DFM (Design for Manufacturing)
 - Taking Manufacturing related requirements into account during design
 - DFM Domains
 - **DFF** (Design for Fabrication): Checks related to plain PCB Manufacturing
 - **DFA** (Design for Assembly): Checks related to Component Mounting
 - **DFT** (Design for Testing): Checks related to Testing
- FloWare
 - Digital Soldermask
 - Edge Plating

DFM – Design for Manufacturing

Design for Manufacturing

- Design for Fabrication
 - Min Shape Width
 - Annular Rings
 - Mask Slivers
 - Mask Island
- Design for Assembly
 - Package Spacing
 - Mechanical Hole to Component
- Design for Test
 - Testpoint to Testpoint Spacing
 - Testpoint to Component Spacing



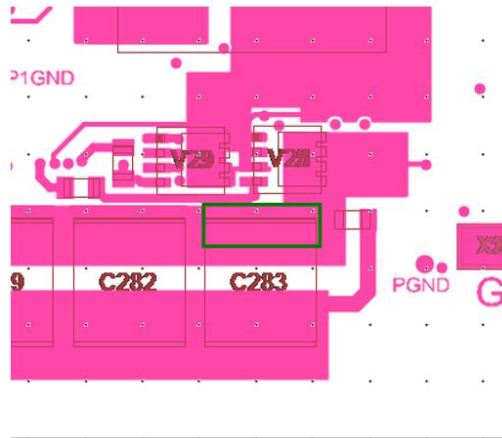
DFM Examples

- Typical examples for manufacturing issues, which can easily be avoided during design
 - Zollner Elektronik AG
 - AT&S
 - Würth Elektronik
 - Cadence
 - Nvidia

DFM Examples Zollner (I)

DFM: Issue solder balls

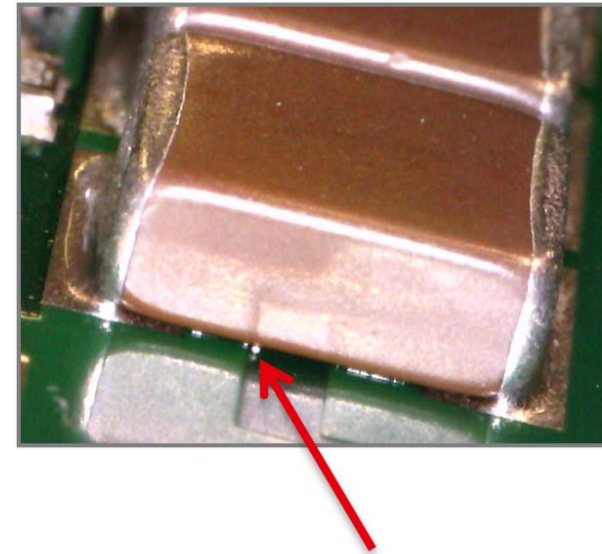
DFM analysis of C283 (C282, C279)



Both toeprints of the component are not placed on an equal sized pad.
The pads are too big for the toeprints.

Source: Zollner Elektronik AG

Reality on board

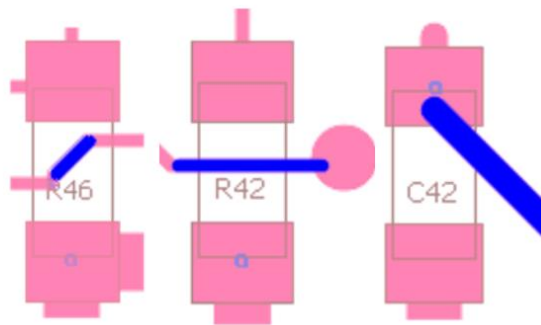


This can cause solder balls under the component!

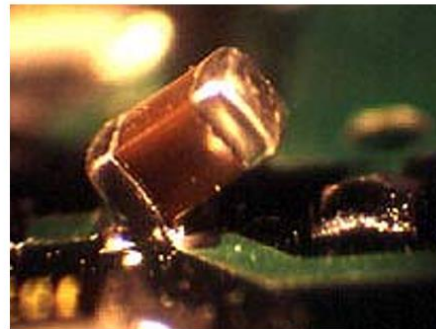
DFM Examples Zollner (II)

DFM: Trace under component

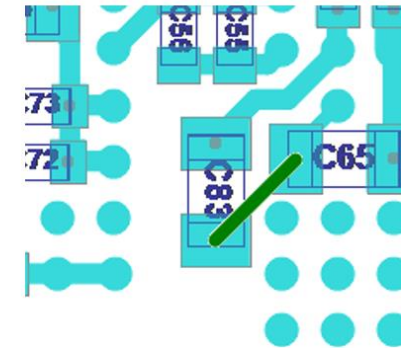
- Lines under zero, stand-off components (such as discrete or resistor pack components, lying close to the board) can interfere with proper placement. Tombstoning or a stand-off can be possible.



General examples for traces designed under component



General example for tombstoning effect

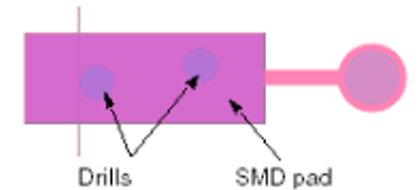


Example for trace under component current design

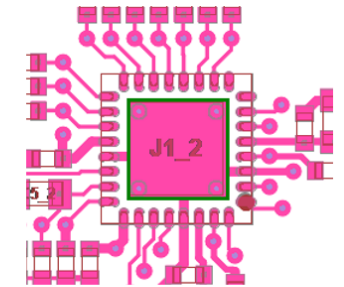
DFM Examples Zollner (III)

DFM: Hole in SMD Pads

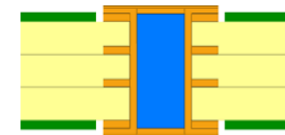
- Reports of holes in SMD pads. Please avoid holes in SMD pads. If there are any, they must be plugged otherwise they should be removed
- For example here in a heatsink landpattern
- If the holes / vias are treated in a proper style it would be no issue any more
- Please care about the IPC-4761 type VII (filled and capped)



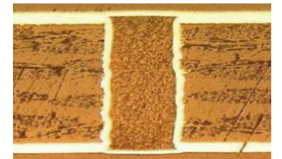
General examples for hole designed in SMD pad



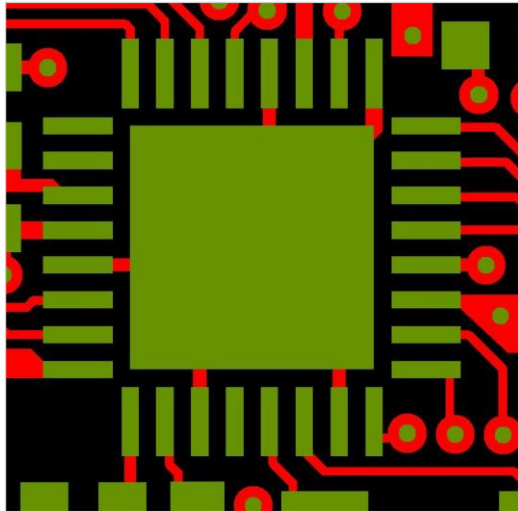
Sketch



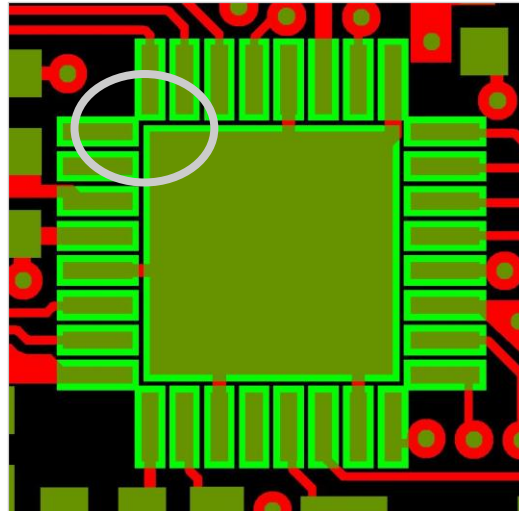
Cross Section



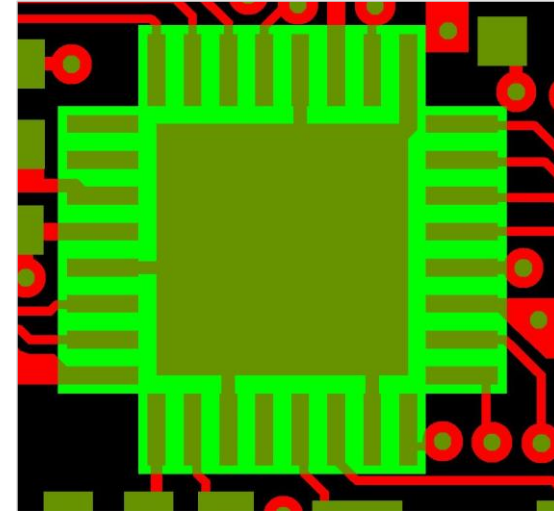
DFM Examples AT&S (I)



Optimal pad / soldermask 1:1

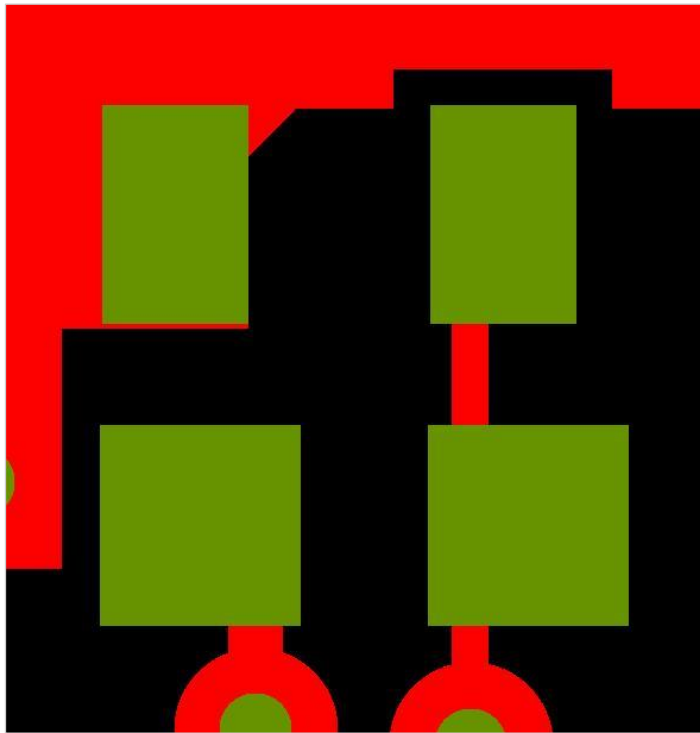


Increased soldermask remaining path too small

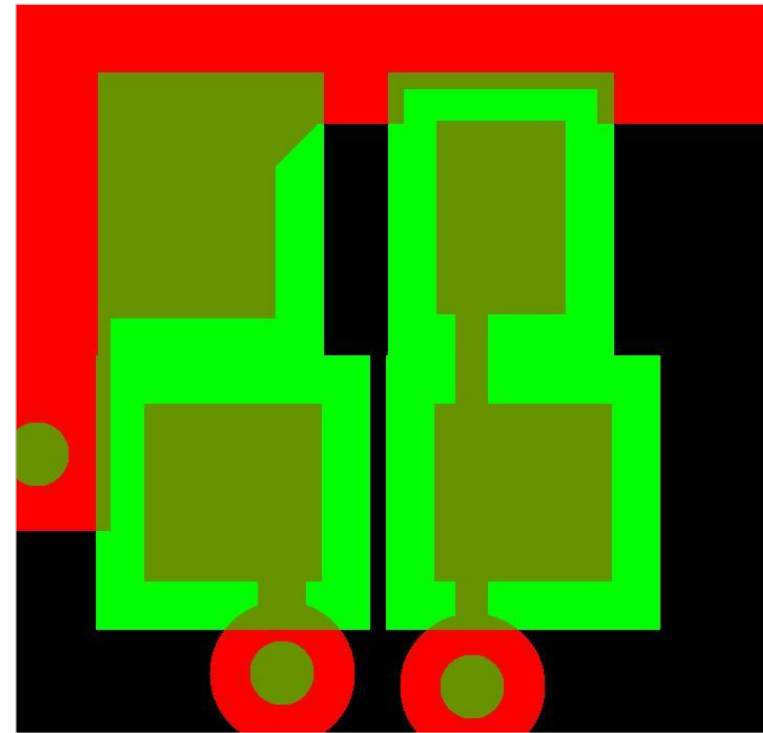


Increased soldermask, no more gap between soldermask pads available

DFM Examples AT&S (II)



Optimal pad / soldermask 1:1

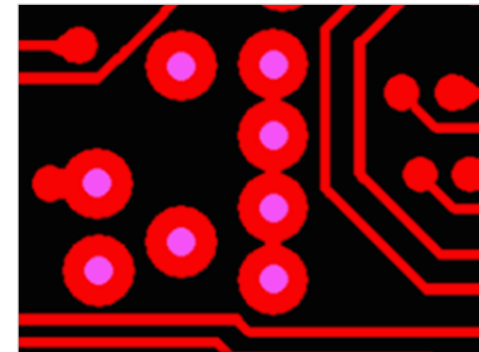
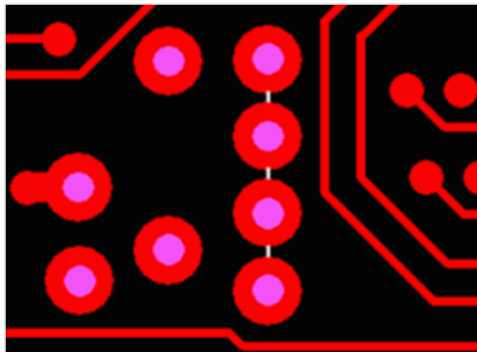


Soldermask opening too large

DFM Examples AT&S (V)

Pseudo Errors During AOI

- Rework on pad connections between pads on the same net
 - Usually areas with more than 200 pads per layer

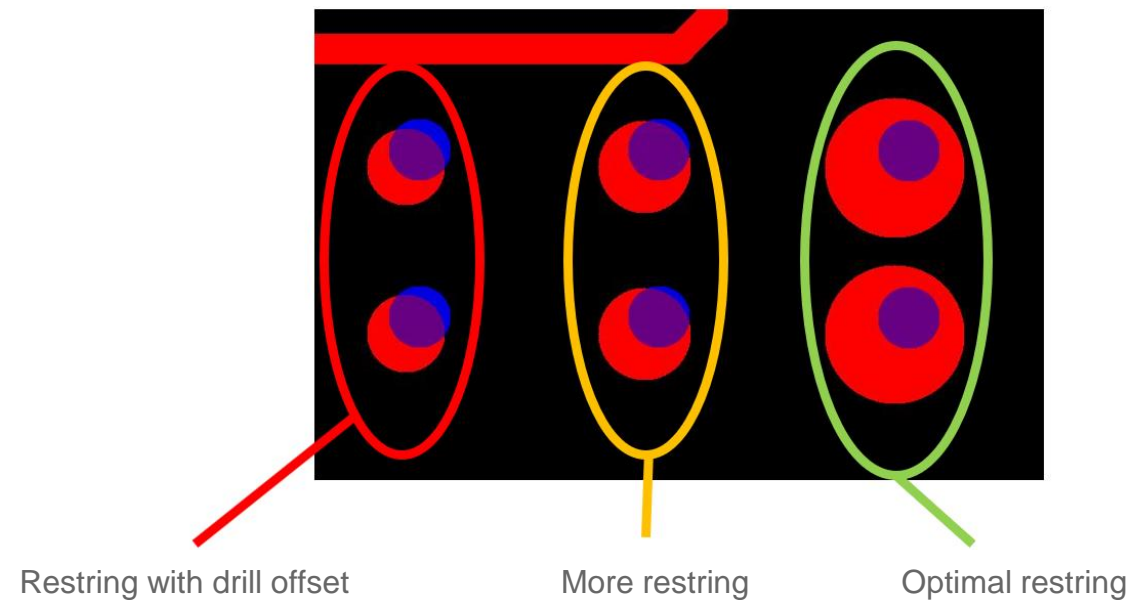


- Areas marks in white represent the pseudo errors during AOI
 - Highlighted areas have $\leq 50\mu\text{m}$ spacing, which is critical during etching process
 - Result: Possible undefined shorts between pads on multiple layers (+200 errors per layer during AOI)
- Additional steps for CAM
 - During preparation, CAM team has to connect each pad individually
 - This rework process and net list modification can take hours for CAM team to complete

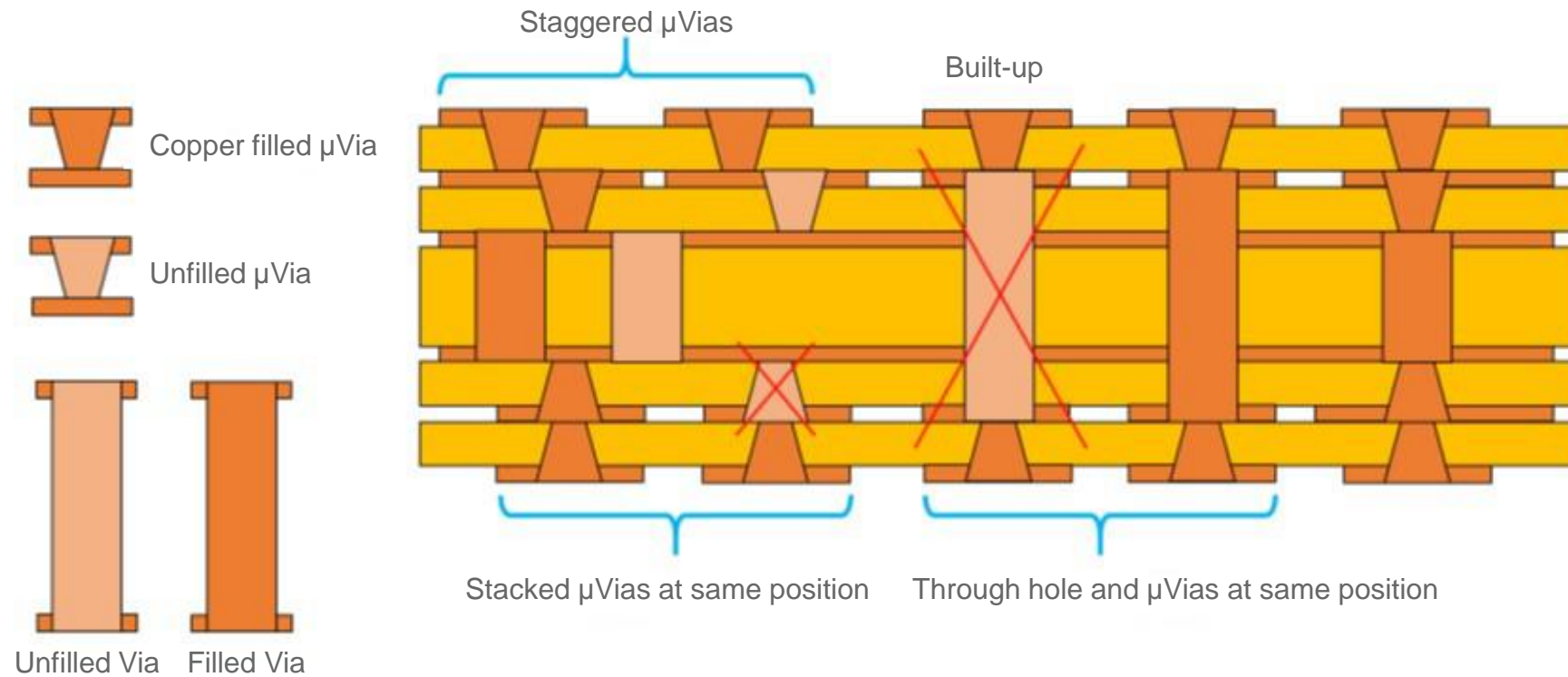
Note: Please check the design (modify if needed) to prevent these errors from occurring!

DFM Examples AT&S (VI)

- Restring requirement for PTH / Via (125 μ circulating)
- Depending the production process
- Annular Ring Check in DFF

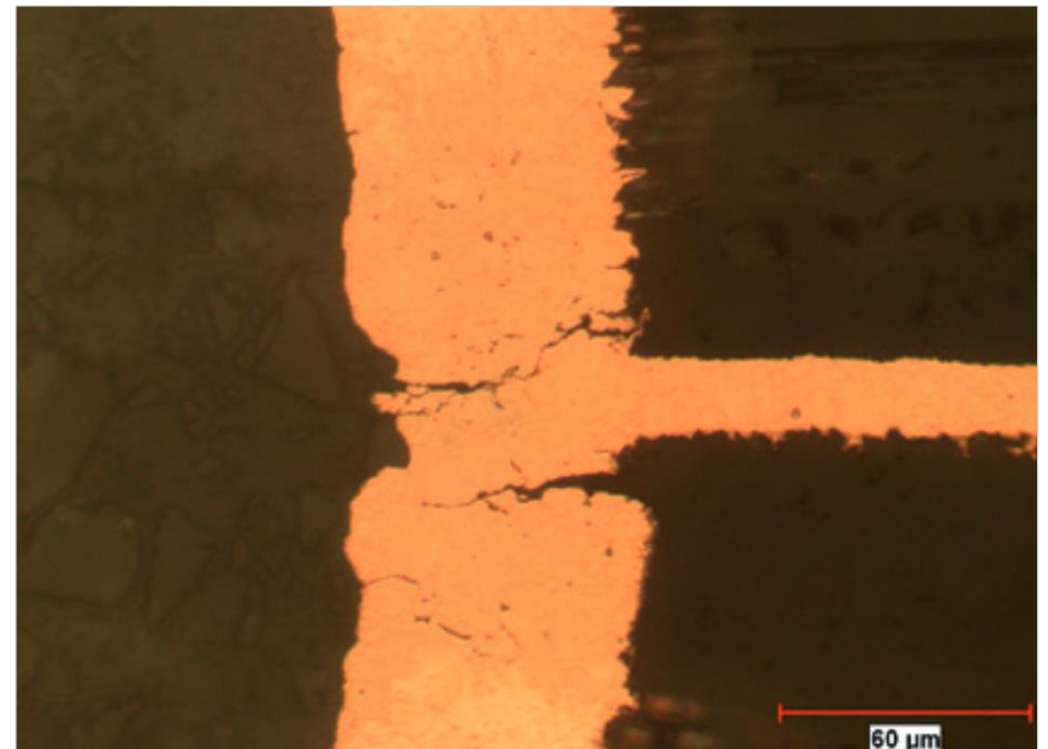


DFM Examples AT&S (VII)



DFM Examples Würth Elektronik (I)

- Hull break due to adverse aspect ratio
 - Different thermal expansion of FR-4 and copper
- Aspect ratio check in DFF



Source: Würth Elektronik

DFM Examples Würth Elektronik (II)

- Aspect Ratio Check

Analysis Modes

Name	On	Off
Mark All Constraints	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
▲ Aspect ratio	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Via	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Plated thru hole	<input checked="" type="checkbox"/>	<input type="checkbox"/>
MicroVia	<input checked="" type="checkbox"/>	<input type="checkbox"/>
Skip via	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Max stacked via count	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Maximum stacked uvias count	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Maximum count of uvias stacked on core via	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Alignment between uvias	<input type="checkbox"/>	<input checked="" type="checkbox"/>
Alignment between uvias stacked on core via	<input type="checkbox"/>	<input checked="" type="checkbox"/>

On-line DRC

OK Cancel Apply Help

Hole Plated Through Hole Aspect Ratio

Checks the maximum aspect ratio for thru hole pin.

Aspect Ratio = Substrate Thickness/Drilled Hole Diameter

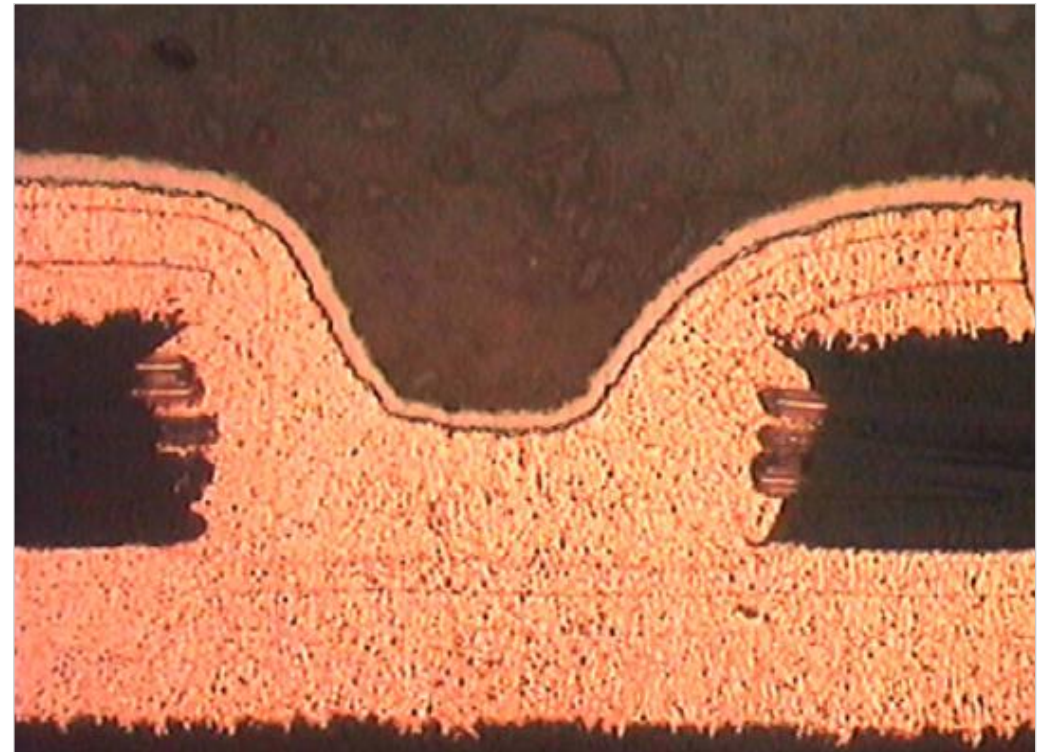
Thru Hole Aspect Ratio = 10:1
(.100"/.010")

Laser Via Aspect Ratio = .5:1
(.003"/.006")

DRC Code: ht
Applicable Objects: DffHoleCSet
Attribute Name: DFFHLS_PTH_ASPECT_RATIO

DFM Examples Würth Elektronik (III)

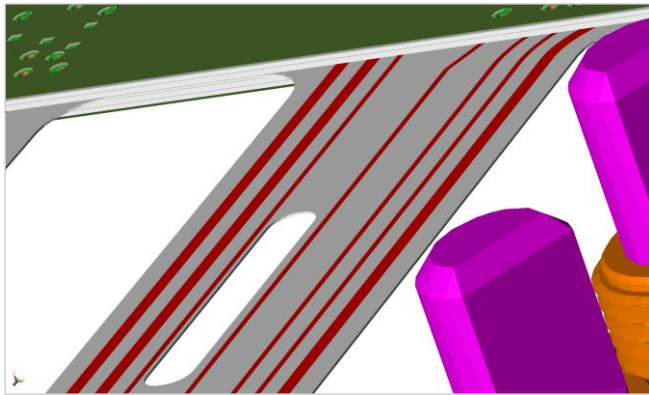
- Solution: Laser drilled microvias
 - Short hulls are not likely to break



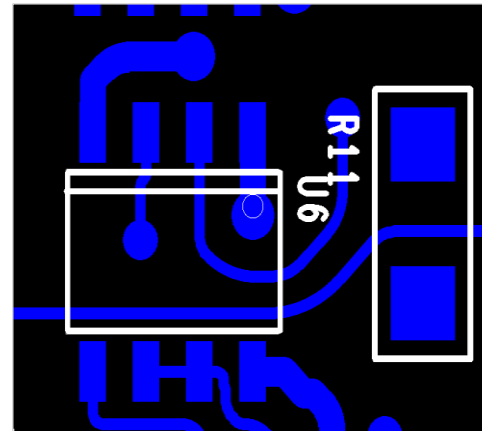
Source: Würth Elektronik

DFF Examples Cadence (I)

- Outline / cutout spacing
 - Trace too close to a cut-out

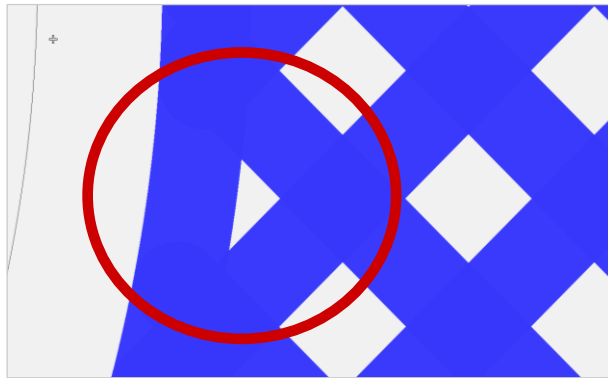


- Silkscreen
 - Silkscreen to silkscreen
 - Silkscreen to pad

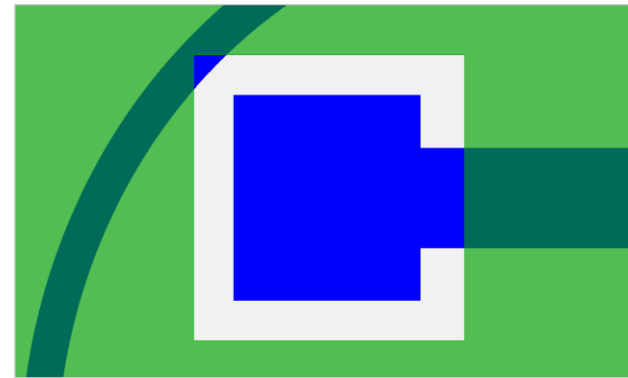


DFF Examples Cadence (II)

- Copper feature
 - Acid trap in a shape

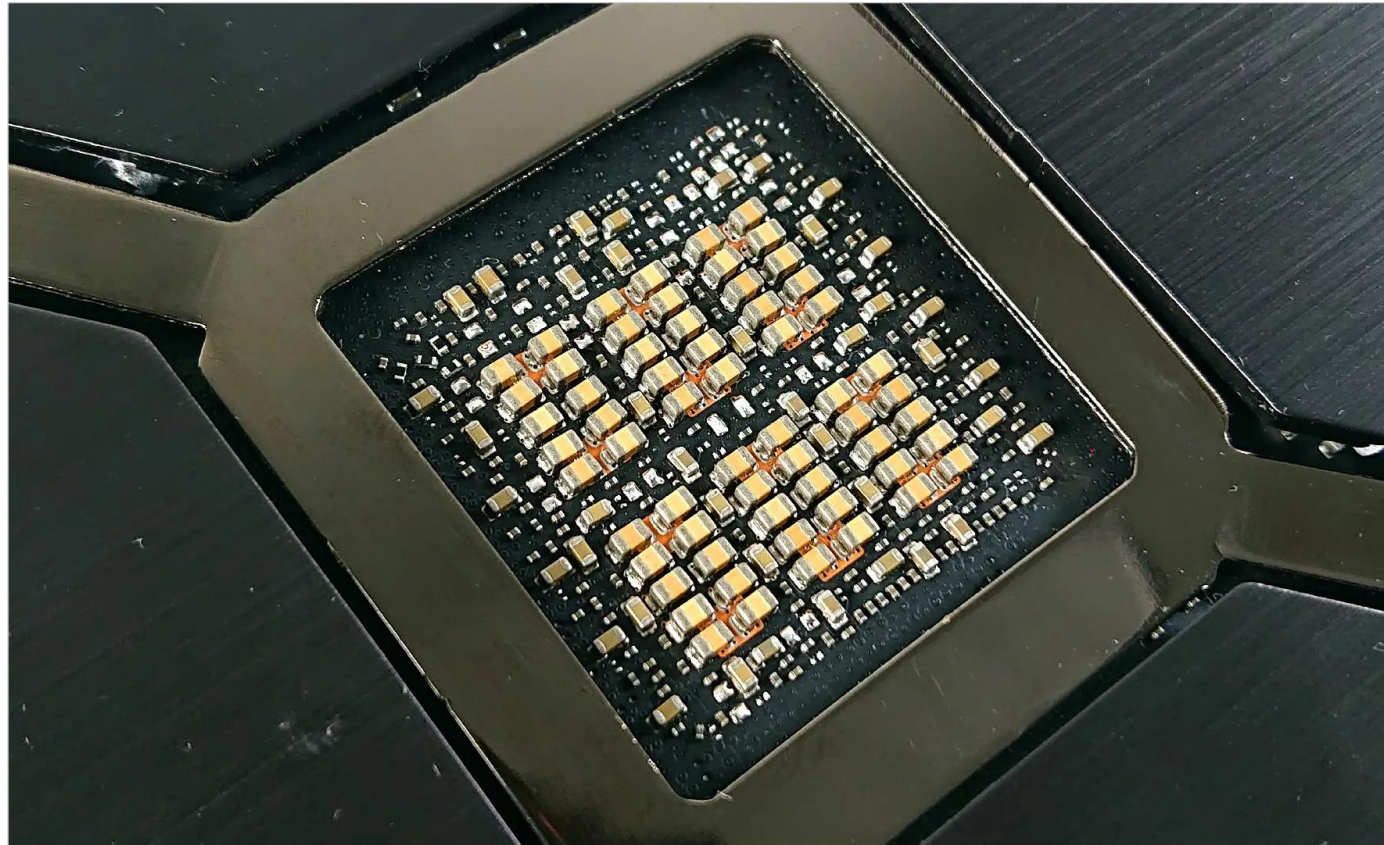


- Soldermask
 - Solder paste wicking
 - Maximum exposed etch in soldermask



GeForce RTX 3000: Stability Problem (I)

- Stability problem due to capacitors under graphic chip



Source: www.heise.de

GeForce RTX 3000: Stability Problem (II)

- Might be a design / manufacturing issue
 - Pad design
 - Copper
 - Soldermask
 - Pastmask
 - Vias in pads
 - Solder process

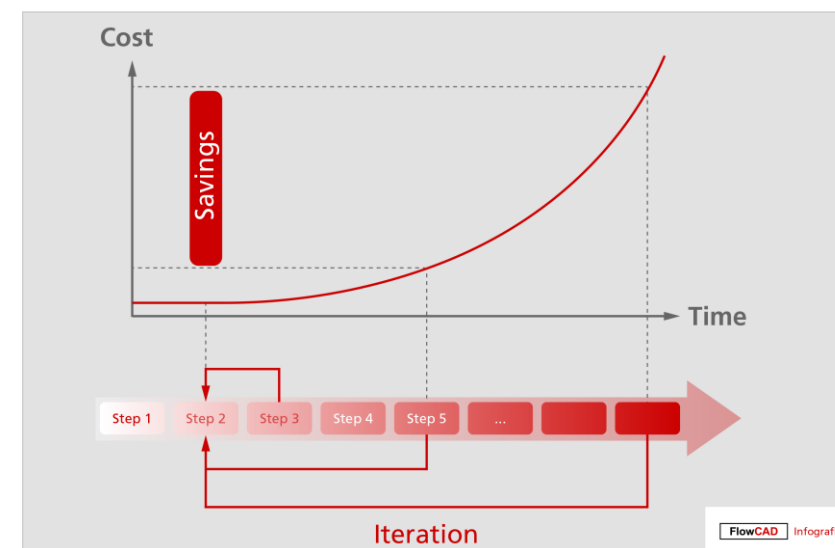


Earlier is Cheaper

- Late discovered errors get more expensive
 - Iterations
 - Prototypes
 - Redesigns
 - Missed market entry
- Avoiding errors by early detection saves costs
 - Signal- and Power-Integrity
 - DFM, DFA, DFT, ...
 - Manufacturing, Assembly and Test
 - Thermal
 - EOL

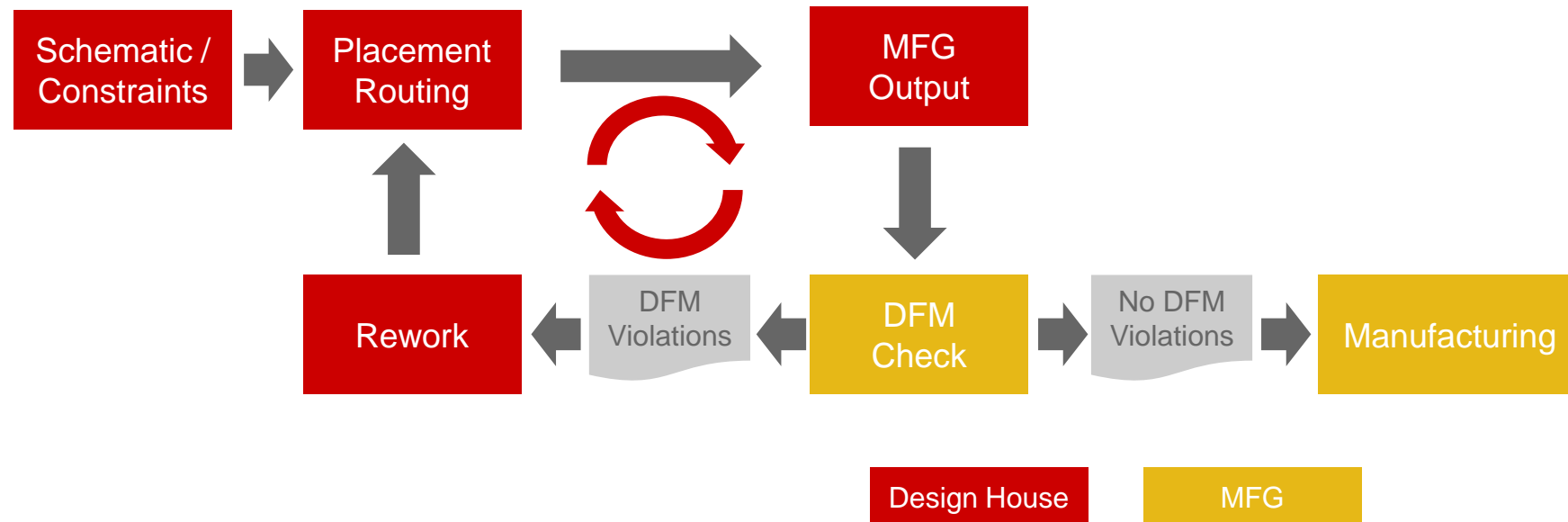
Cost of different timing:

Alternate circuit idea	1 €
Changes in schematic	10 €
Changes in PCB Layout	100 €
Changes after CAM / DFM check	1.000 €
Redesign after prototype	10.000 €
EOL-Redesign after market introduction	100.000 €
World wide recall due to malfunction	1.000.000 €



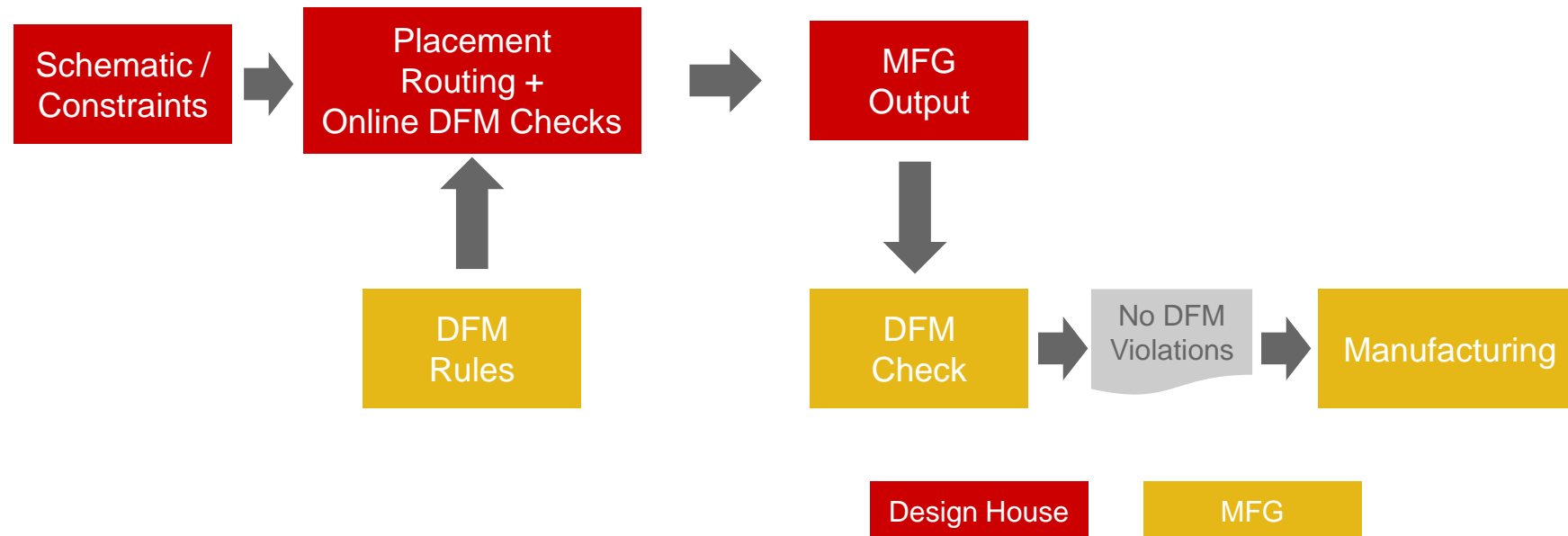
Traditional PCB Design Flow

- DFM Checks are done after design is finished
- Time-consuming design cycles in case of manufacturing issues
- Design loops required to guarantee manufacturability



In-design DFM Checks Flow

- First time right
 - By using production proved DFM rules from manufacturing
 - By online DFM rules check during design
- Manufacturing related checks are online during PCB Design
 - No re-spins required

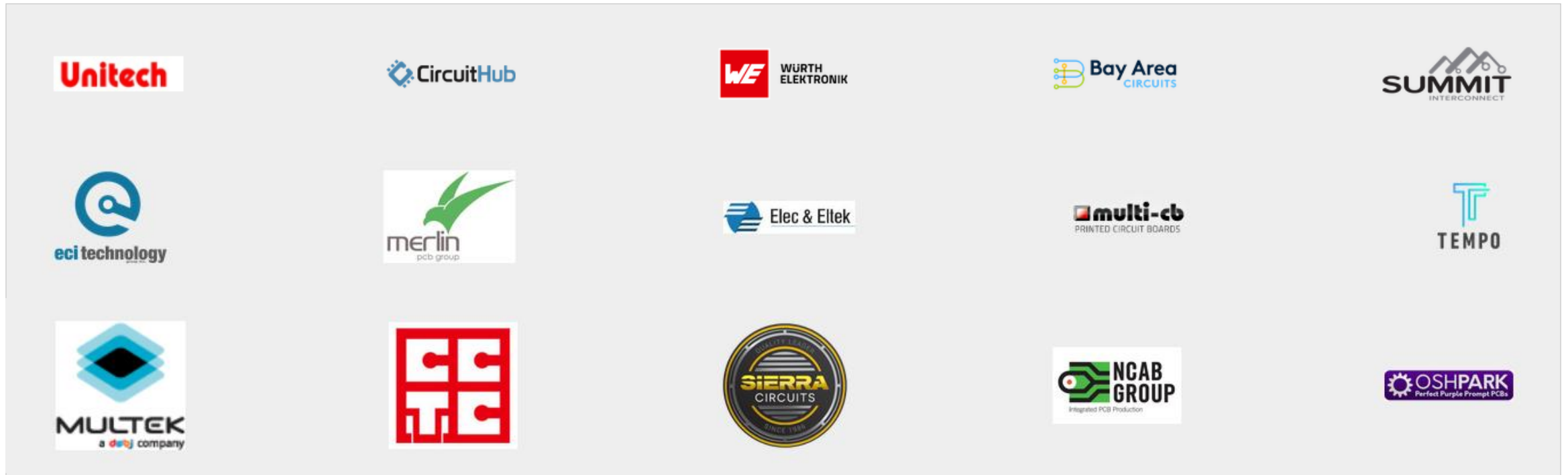


DesignTrue DFM Ecosystem

- On-line Rule Description
 - Describes rule intent
- Inherited Values
 - Major categories populate children of rule
 - Allows independent rule entry definition
- Download completed sets
 - Uses web tool download location
 - No data stored on server, download to client

DFM Portal

- Cadence offers DFM Portal to request DFM rules at PCB Manufacturer
 - Production proven rules
 - No need to enter manually



Web-based Rules Request

- PCB Designer can request rules sets in web portal
 - https://pcb.cadence.com/dfm_customer

The screenshot displays the Allegro DesignTrue DFM Rule Editor web portal. The interface is organized into several sections:

- File Setup:** Includes fields for File Name, Units (Mils), Accuracy (2), Site (CH01), Manufacturing Class (IPC Class 2), Design Technology (Rigid), Minimum Finished Hole Size, Expected Minimum Line Width, and Expected Minimum Line to Line Spacing.
- Options:** A grid of checkboxes for various manufacturing options, including Minimum BGA Pin Pitch, Minimum BGA Pad Size, Micro Via, Blind/Buried Via, Back Drill, Embedded/Coil, Non Conductor (Outline, Mask), Silkscreen, Conductors (checked), and Layers/Weight (External, Internal, Plane).
- Units and Accuracy:** A footer bar shows Units: Mils and Accuracy: 2.

The bottom of the page contains a footer with legal information and social media links.

Web-based Rules Description

- Manufacturer can enter rules in web portal
 - https://pcb.cadence.com/dfm_vendor

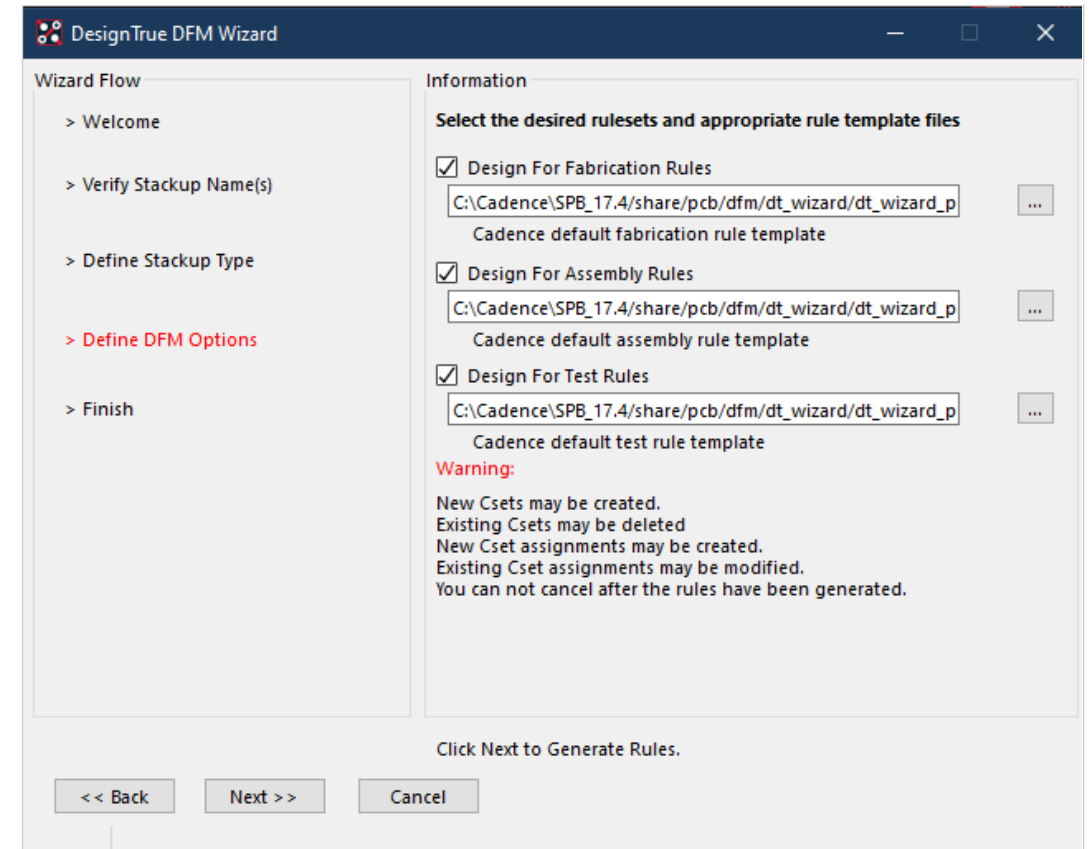
The screenshot displays the Allegro® DesignTrue DFM Rule Editor web portal. The interface is divided into several sections:

- Header:** cadence logo, Allegro® DesignTrue DFM Rule Editor, and user information (Edward Acheson).
- Navigation:** Tabs for File Setup, Annular Ring Rules, Holes Rules, Copper Features Rules (selected), and Copper Spacing Rules.
- Search:** A search bar with a magnifying glass icon and a 'Reset All' button.
- Left Sidebar:** A tree view showing rule categories:
 - Copper Features
 - Minimum
 - Line width
 - Text line width
 - Shape width(positive)
 - Void opening(positive)
 - Line width ratio
 - Text line width ratio
 - Void Slivers
 - Maximum
 - Shape into pad ratio
 - Line into pad ratio(SMD)
 - Line into pad ratio(Thru Hole)
 - Flex
 - Min radius on all trace corners
 - Max solid fill on shapes
 - Missing trace tapers
 - Missing pad fillets
 - Missing T fillets
 - Antenna
 - Traces
 - Via
 - Thermal(positive)
 - Isolated thermal
 - Min spoke count
 - Min spoke width
 - Max spoke width
 - Min air gap
 - Thermal(negative)
 - Isolated thermal
 - Min spoke count
 - Min spoke width
 - Max spoke width
 - Min air gap
 - Acid traps
 - Minimum angle
 - Minimum area
 - Plating
 - Plating in pin
 - Plating in via
- Main Content Area:**
 - Selected Rules:** A table listing rules with columns for Rule, Etch Value, and Description.

Rule	Etch Value	Description
Minimum ▶ Line width	5.00 mil	Copper Features: Minimum Line Width
Minimum ▶ Text line width	5.00 mil	Copper Features: Minimum Text Line Width
Minimum ▶ Shape width(positive)	5.00 mil	Copper Features: Minimum Shape Width(Positive)
Minimum ▶ Void opening(positive)	4.00 sq mil	Copper Features: Minimum Void Opening(Positive)
Minimum ▶ Line width ratio		
Minimum ▶ Text line width ratio		
Minimum ▶ Void Slivers	6.00	
Maximum ▶ Shape into pad ratio	2.00	
Maximum ▶ Line into pad ratio(SMD)	2.00	
Maximum ▶ Line into pad ratio(Thru Hole)	2.00	
Flex ▶ Min radius on all trace corners	12.00	
Flex ▶ Max solid fill on shapes		
Flex ▶ Missing trace tapers	On	
Flex ▶ Missing pad fillets	On	
Flex ▶ Missing T fillets	On	
Antenna ▶ Traces	On	Copper Features: Antenna traces
Antenna ▶ Via	On	Copper Features: Antenna via
Thermal(positive) ▶ Isolated thermal	On	Copper Features: Isolated thermal
Thermal(positive) ▶ Min spoke count	4.00	Copper Features: Min Spoke count
Thermal(positive) ▶ Min spoke width	8.00 mil	Copper Features: Min spoke width
Thermal(positive) ▶ Max spoke width	10.00 mil	Copper Features: Max spoke width
Thermal(positive) ▶ Min air gap	6.00 mil	Copper Features: Min air gap
Thermal(negative) ▶ Isolated thermal(Neg)	On	Copper Features: Isolated thermal(Neg)
Thermal(negative) ▶ Min spoke count	2.00	Copper Features: Min Spoke count(Neg)
Thermal(negative) ▶ Min spoke width	8.00 mil	Copper Features: Min spoke width(Neg)
 - Modal Window:** A pop-up window titled "Minimum Line Width" showing a 3D model of a PCB trace and the description: "Checks minimum width that is allowed on a line segment in etch/conducting layer." The modal also includes a "View" button.
- Footer:** File: CDN6_CHEL_MC2_DTRigid_COND_EXT0.5.tctx, Units: Mils, Accuracy: 2, and social media links.

DFM Wizard

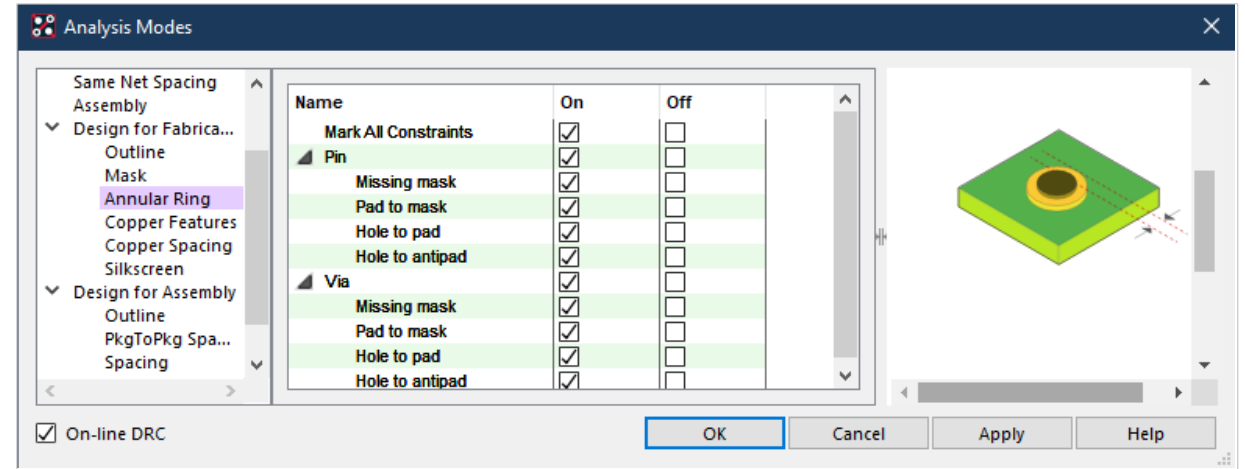
- Automated import of rules sets
- Wizard guides through import process
- Automated adaption to stackup and technology



DFF and DFA Checks

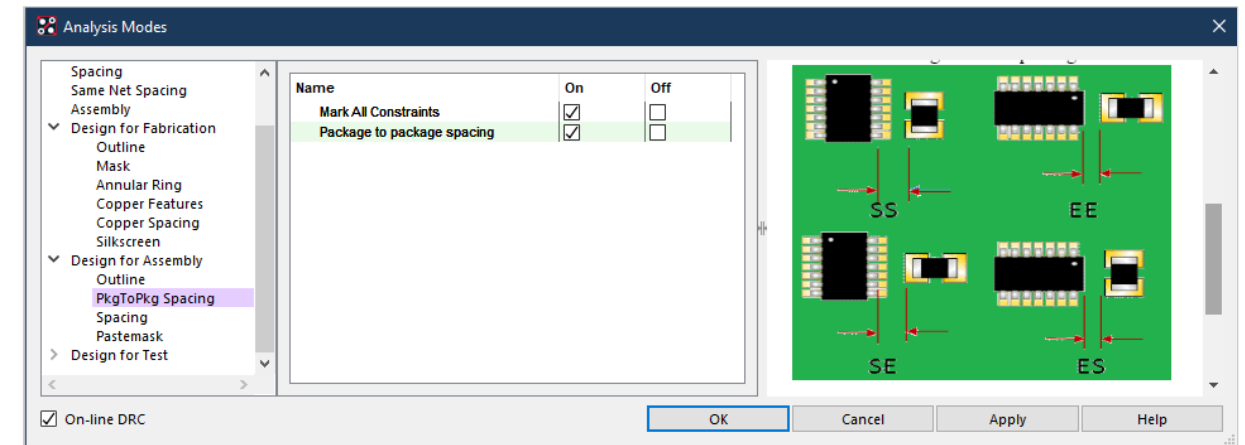
- DFF Constraints

- Outline (cutout)
- Mask
- Annular ring
- Copper spacing
- Silkscreen

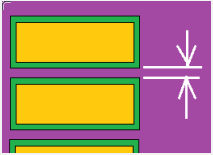
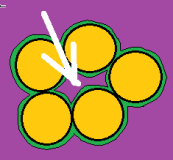
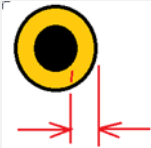
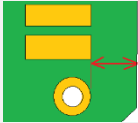
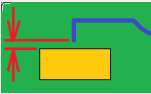


- DFA Constraints

- Outline
- Spacing
- Pastemask
- Fiducial

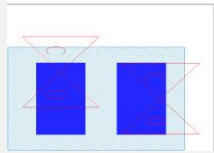
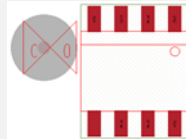
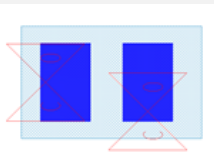
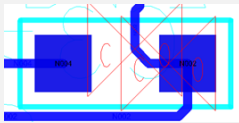
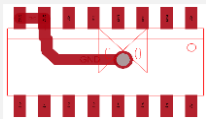


Fabrication DRC Examples (DFF)

Rule	Description	Usage	Picture
Mask Sliver	This specifies the minimum width of a mask where the potential for mask material deposited may become delaminated from the PCB substrate. Checks are based on the mask layer being the standard negative image use model	Non-Etch	
Mask Islands	This specifies the minimum square area of mask material, where if the mask area is too small, may delaminate from the PCB. Checks are based on the mask layer being the standard negative image use model	Non-Etch	
Pin Hole to Pad	The minimum distance of the pin padstack hole to the outermost edge of the pad geometry	Etch	
Outline to Pin Pad	The clearance between any Pin pad edges to the DESIGN_OUTLINE geometry	Etch, Non-Etch	
All Pin Pads	This specifies the minimum allowable distance of any silkscreen geometry to the edge of a pin pad	Non-Etch	

Total Number of DFM Rules: ~ 2.500

Assembly DRC Examples (DFA)

Rule	Description	Usage	Picture
Pastemask to Outline	Checks the space between the DESIGN_OUTLINE geometry and the edge of any PASTEMASK geometry. Any measured value smaller than the rule value is reported as a DRC. Paste mask layers must be defined in the design Cross-section	Non-Etch	
Component body to tooling hole	Defines the minimum allowable distance between edge of a component instance to a tooling hole	Etch	
Pastemask to Pad	Checks the space between the edge of any PASTEMASK geometry and to component's SMD pin pad	Non-Etch	
Trace under Component	Defines the list of package symbols where traces are not permitted under the component boundary	Etch	
Large Via under component	A Yes value displays a DRC for any large vias under any component body. A No value turns the check off for this rule	Etch	

Total Number of DFM Rules: ~ 2.500

FloWare

FloWare Features

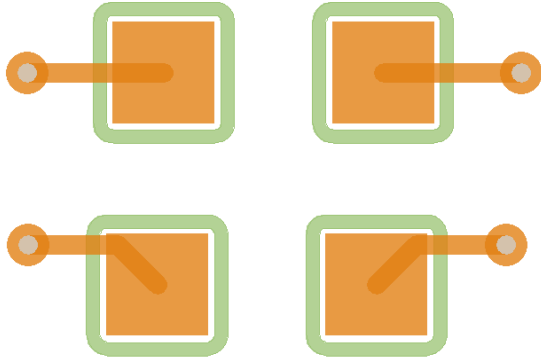
- General purpose utilities
 - Functions not in standard tool yet
 - Not written for one specific customer
 - Everybody should benefit
- Easy installation
 - Also casual users must be able to install FloWare
 - No variables
 - Menus will be created automatically
 - Integrates perfectly into existing customizations
- Documentation
 - Full documentation is provided for every module

FloWare Modules Overview

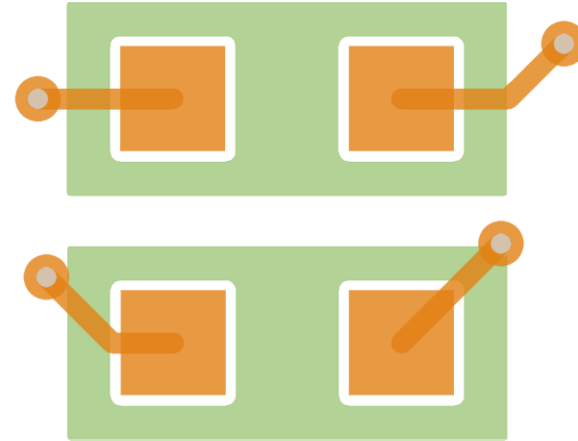
- Advanced Mirror
- Advanced Testpoint Check
- Anti Tamper Mesh PCB
- AOI Check
- Assign Net to Via
- Barcode Generator
- Batchplot
- CAF-DRC
- Change Width
- Class Color
- Cleanliness Check
- Coil Designer
- Contour Place
- Cross Copy
- Cross Section Generator
- Custom Variables
- Design Compare
- **Digital Soldermask**
- Drafting Utilities
- Drawing Designer
- Drawing Size
- Drawing View Manager
- **Edge Plating**
- FPGA Utilities
- Highlight Dummy Pins
- IBIS Prototype Modeler
- Label Generator
- Label Tune
- Mask Generator
- NC Panel Route
- Net Color View
- Padstack Finder
- Padstack Usage
- Panelization
- PCB Library Plot
- Polar Grid Utilities
- Post Processing
- Push to Grid
- Quick Symbol Edit
- Replace Via
- Shape Utilities
- Shield Generator
- Shield Routing
- Silkscreen
- Snap Generator
- SVG Export
- Synchronize Testprep
- Variant 3D
- Variant Assembly
- Variant BOM
- Z-DRC

Digital Soldermask

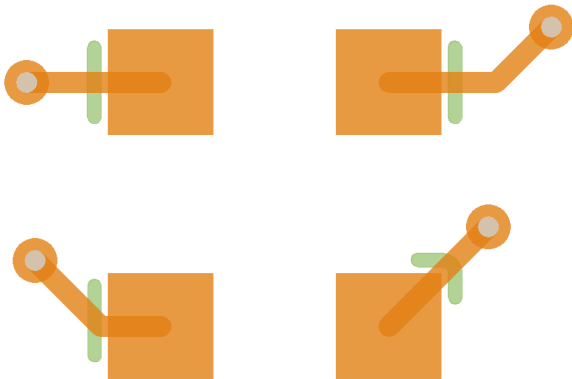
Pad box



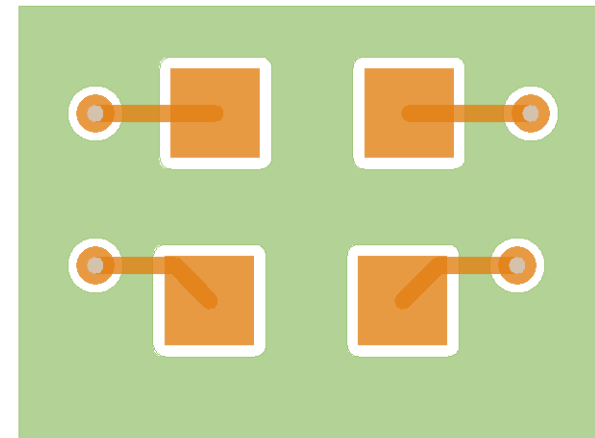
Component boundary



Trace mode

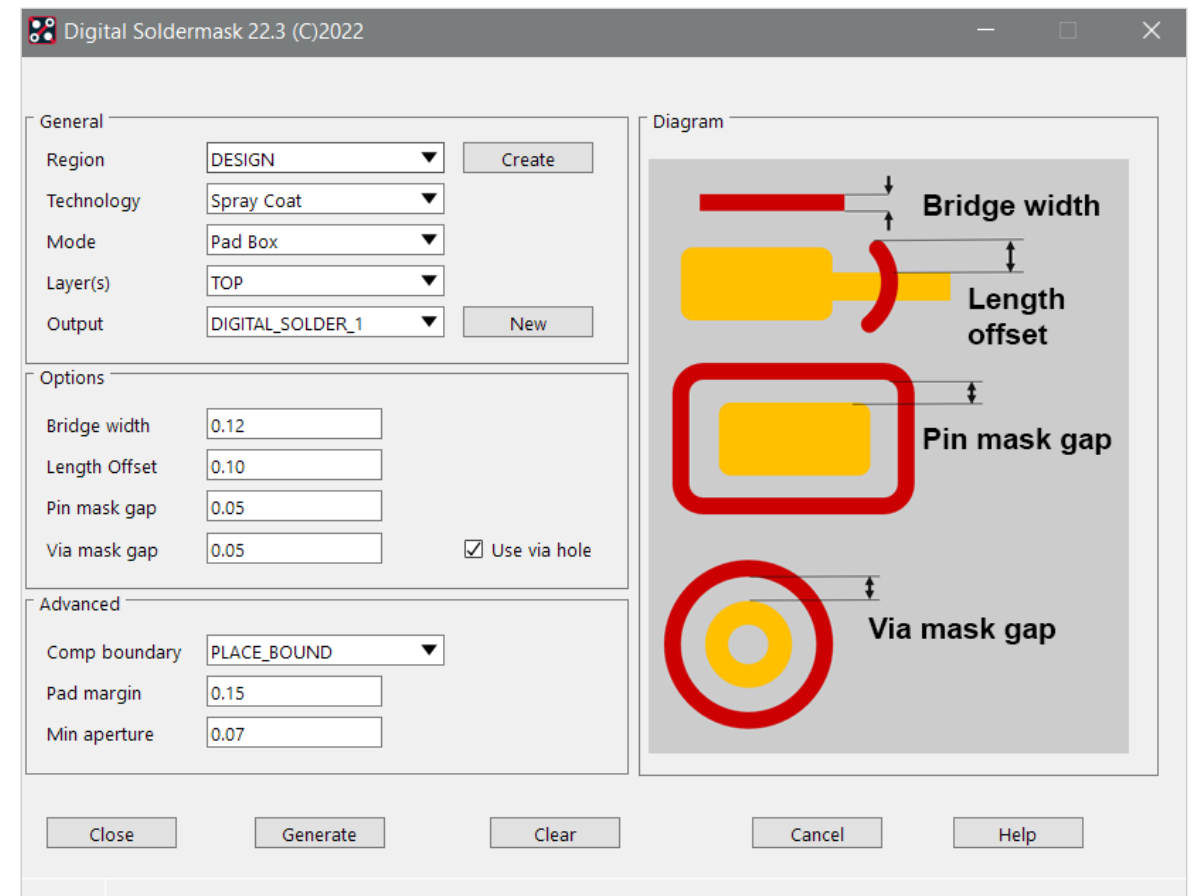


Soldermask region



Digital Soldermask

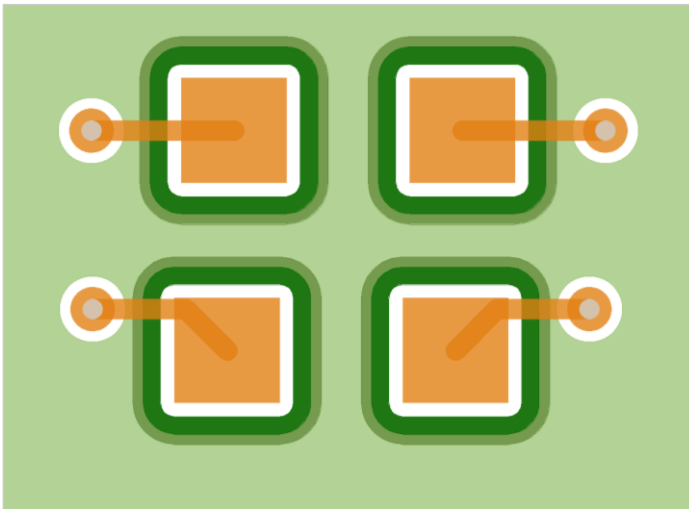
- Developed together with Würth Elektronik
- Various modes
 - Pad ring / box
 - Trace mode
 - Component mode
 - By region
- Parameters
 - Bridge width
 - Pin, via gap
 - Length offset
 - ...



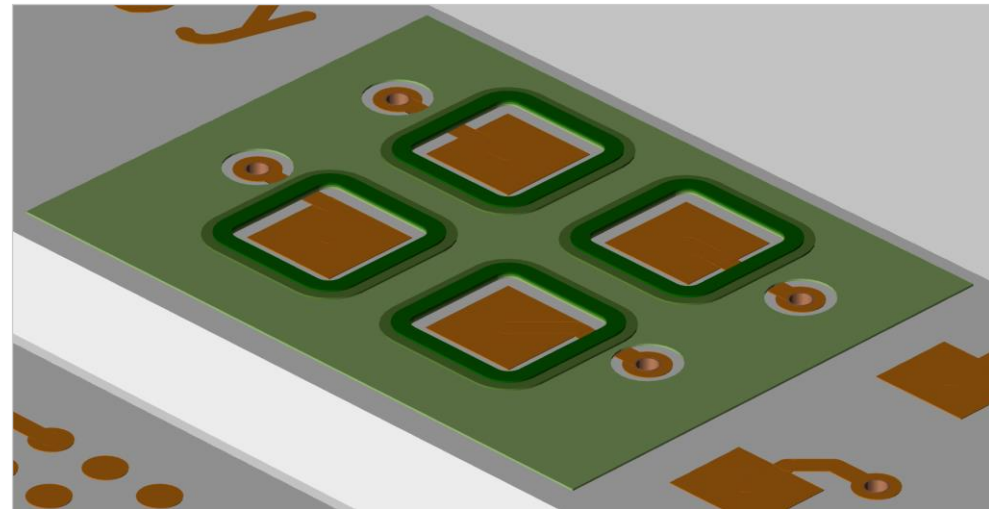
Digital Soldermask

- Techniques can be combined and used to create multiple masks on separate layers, accounting for mask thickness requirements

2D



3D canvas

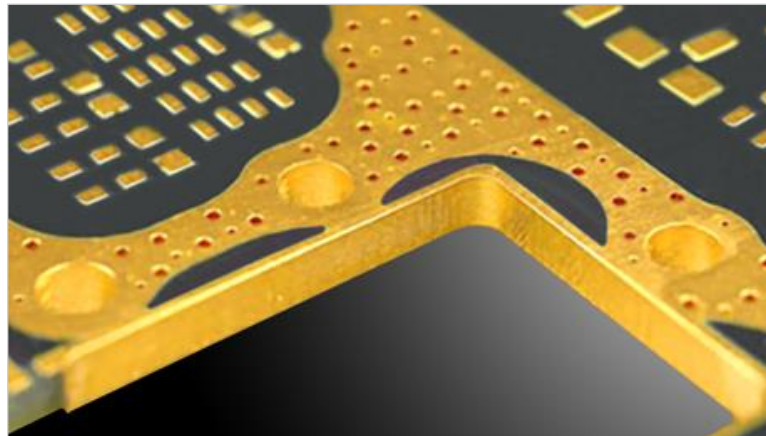


- In example above:
 - Soldermask region on Digital_Soldermask_1_TOP
 - Pad box on Digital_Soldermask_2_TOP
 - Pad box on Digital_Soldermask_3_TOP



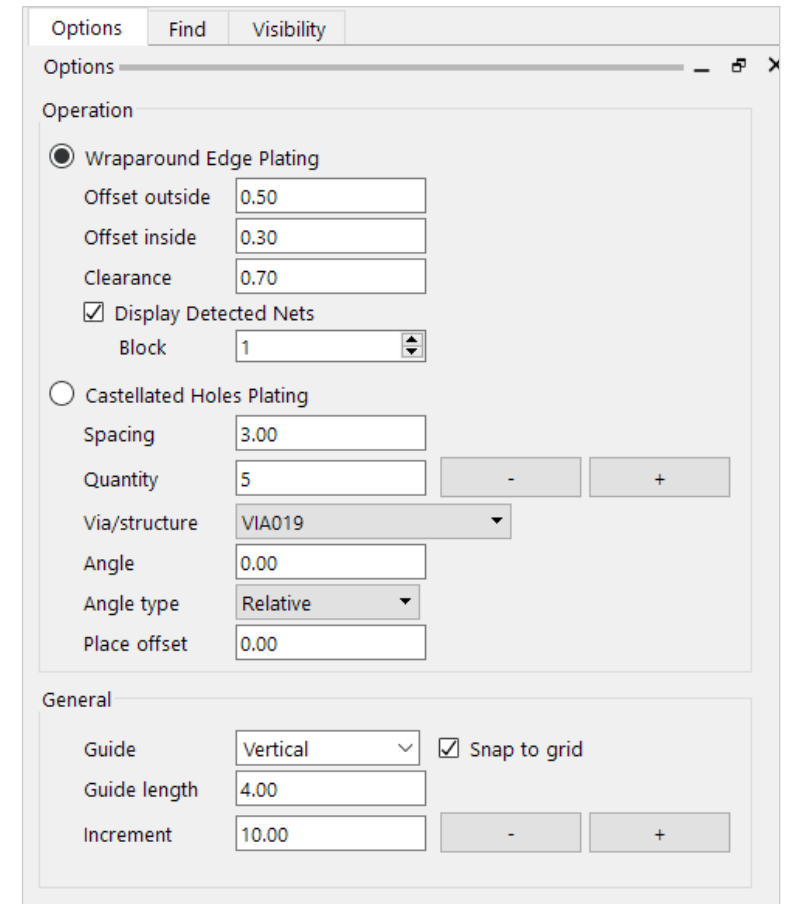
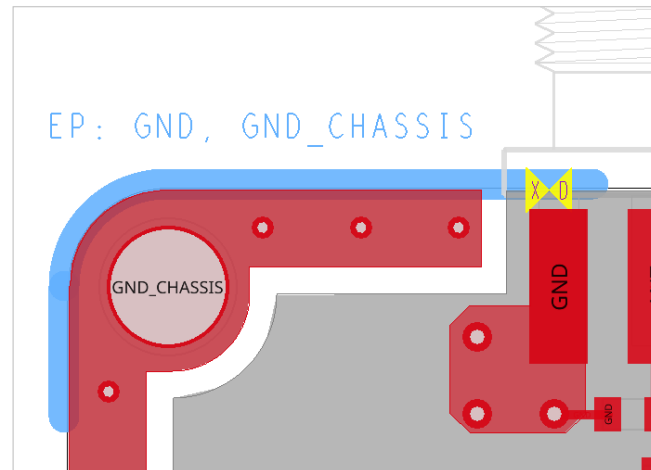
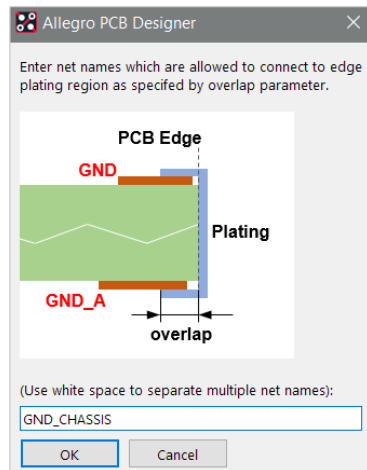
Edge Plating

- Edge plating is a plated conductive material on the edge of a PCB where in normal instances, only dielectric material is exposed
- This plated conductive material may be used for many functions
 - Improve current carrying across multiple layer of a PCB
 - Edge connection protection
 - Board to case grounding
 - EMC signal integrity
 - Heat management
- Two forms of Edge Plating
 - Wraparound (Side) Plating
 - Castellated Holes



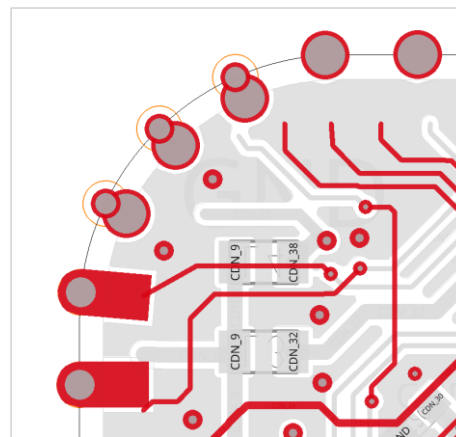
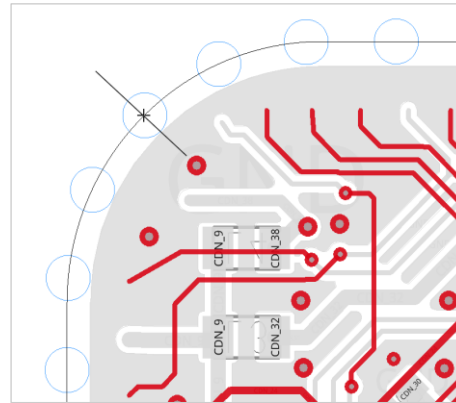
Edge Plating: Wraparound (Side)

- Define plating sections interactively
- Net assignment
- Connectivity Check
- DRC Clearance Check
- Net Short support



Edge Plating: Castellated Holes

- Define locations interactively along outline supporting
 - Spacing
 - Quantity
- Objects supported
 - Vias
 - Via structures
 - Symbols
 - Electrical components
- Placement parameters
 - Alignment with outline (relative, absolute)
 - Offset from outline



Options	Find	Visibility
Options		
Operation		
<input type="radio"/> Wraparound Edge Plating		
Offset outside	0.5000	
Offset inside	0.3000	
Clearance	0.7000	
<input checked="" type="checkbox"/> Display Detected Nets		
Block	1	
<input checked="" type="radio"/> Castellated Holes Plating		
Spacing	3.0000	
Quantity	5	- +
Via/structure	VIA_C500_D200	
Angle	0.0000	
Angle type	Relative	
Place offset	0.0000	
General		
Guide	Vertical	<input checked="" type="checkbox"/> Snap to grid
Guide length	4.0000	
Increment	10.0000	- +

FloWare Link Tips

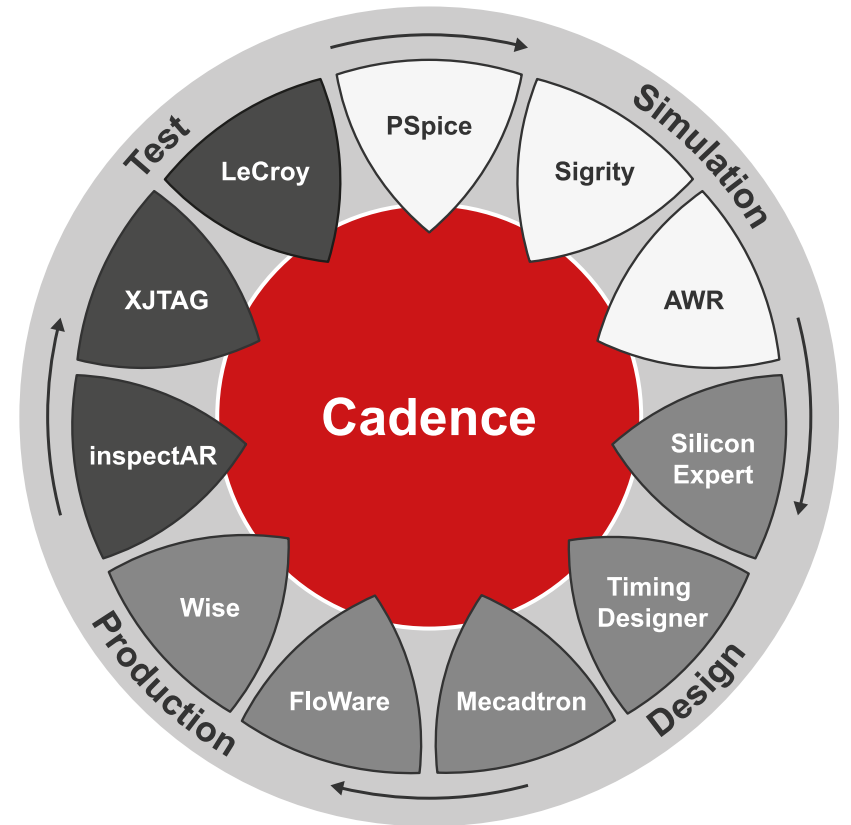
- [Overview of All Available FloWare Modules](#)
- [Free Trial](#)
- [FloWare Datasheet](#)
- [FloWare Detailed Description](#)
- [Videos @ YouTube](#)



Products / Solutions for Electronic Designers

Solutions

- PCB Layout
- PSpice-Simulation
- SI- and PI-Simulation
- EMI and Antenna Simulation
- Timing Analysis
- Thermal Simulation
- 3D mCAD-eCAD Integration
- CAM Verification
- Boundary Scan Test
- Protocol Analysis
- Electronic Data Management
- PLM and ERP-Connection



Focus on Customer Satisfaction

Sales

- Fair, competent advice
- Long term solutions

Support

- Hotline, Fastviewer
- Survey

Service

- PCB Design Services
(Layout, Simulation, Migration)

Training

- Trainings center, on-site
- Workshops



Contact us / Kontakt zu FlowCAD

Please do not hesitate to contact us.

Für weitere Fragen und Informationen stehen wir gerne zur Verfügung.

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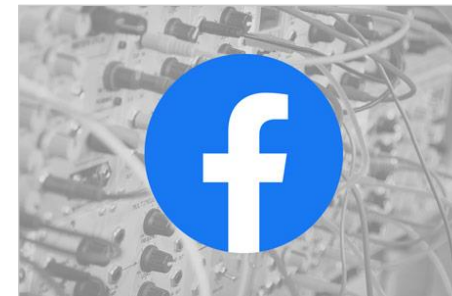
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