Microtec Nord 2023 14. September 2023, Heide

Niedertemperatur-Weichlöten in der Elektronikfertigung - zuverlässige Lote für die industrielle Anwendung?

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1

Inhalt

- Vorstellung ISIT
- Motivation für die Einführung niedrig schmelzender Lotlegierungen
- Ausgewählte Komponententypen
- Produktionsprozesse im direkten Vergleich von SAC und LTS Loten
- Ergebnisse aus Zuverlässigkeitstest:
  - T-Schock -40°C/85°C, Drop Test, Scherfestigkeit
  - Analytik: optisch, Röntgen, Querschliffe, elektrische Tests im 0h-Zustand und nach TCT, InSitu-Monitoring
- Zwischenfazit
- Herausforderung und Ausblick

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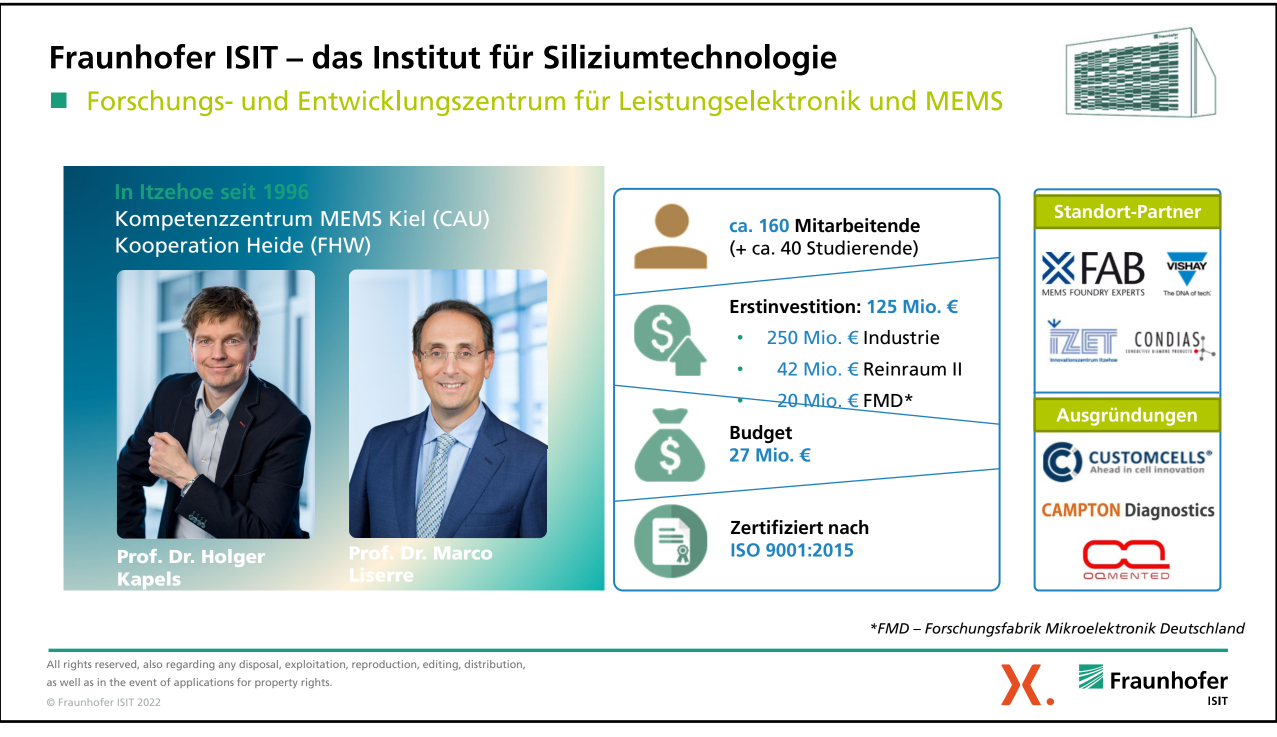
2



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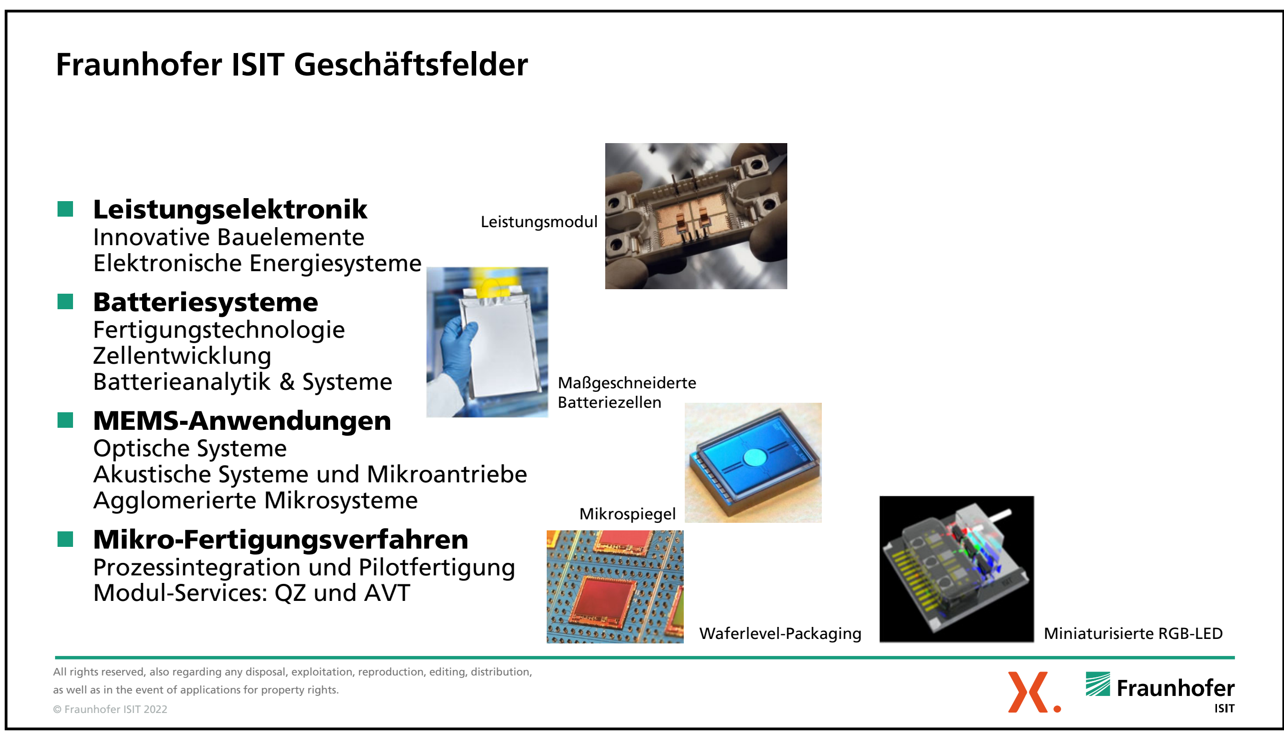

4

Modul-Services – Qualität, Zuverlässigkeit und AVT elektronischer Baugruppen und Komponenten

Fortschrittliche Fehleranalyse ist die Grundlage für Innovation, Geschwindigkeit, Qualität, Zuverlässigkeit und garantierte Funktion über Lebensdauer

- Material- und Schadensanalysen, Kontaminations-, Korrosions- und Rückstandsuntersuchungen
- Bewertung der Herstellungsqualität nach Industriestandards
- Zuverlässigkeits- und materialkundliche Bewertung

Whisker-, Tombstone- (oben) und Rissbildungen (unten) an elektronischen Bauelementen

- Einführung neuer Technologien
- Prototyping und Vorserienfertigung
- Prozessoptimierung, Bauteil- und Materialqualifizierung (Lötwärmebeständigkeit, Lotpastenbewertung, u.a.)
- Rework komplexer Baugruppen
- Seminare und In-House-Schulungen

ISIT SMT-Testbord

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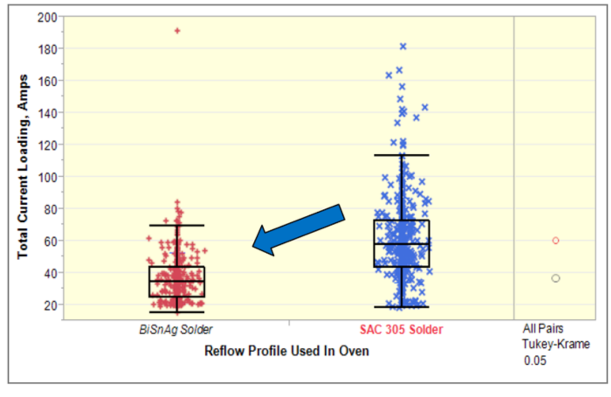
Motivation Energieverbrauch

Reduktion durch Einsatz von BiSnAg Lot ggü. SAC Lot



40% Reduction in Electricity Consumption

Measured Parameter	SAC Reflow	BiSnAg Reflow
Current (RMS), amps	60.4	36.7
Power (Average), Kilowatts	29.3	17.8

Quelle: Intel

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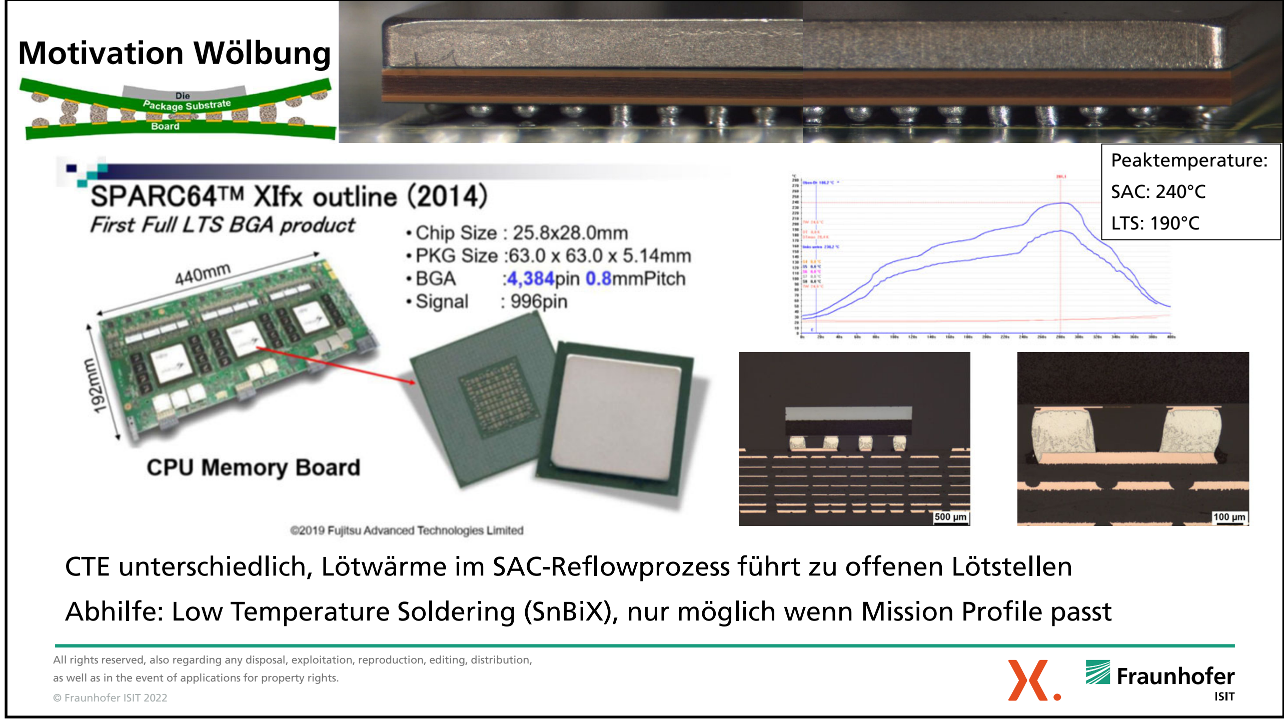

7

Entwicklung von Niedertemperaturloten

Sn-Bi Low Temperature Solder Reliability Performance Evolution

Current Generation

Eutectic Sn-Bi → 2015 → **Sn-Bi-Ag** → 2017 → **Sn-Bi + Dopants "Ductile" LTS** → 2019 → **Sn-Bi + Dopants "Ductile+" LTS**

Eutectic Sn-Bi
- Well documented reliability marginalities – drop & T/C
- Extensive industry experience, common use in durable goods
- Large industry supply base

Sn-Bi-Ag
- Improved performance vs. eutectic Sn-Bi
- Capable of meeting board & system level requirements
- Fails component level requirements

Sn-Bi + Dopants "Ductile" LTS
- Improved performance vs. Sn-Bi-Ag
- Capable of meeting component level requirements
- Bi % 50-58%

Sn-Bi + Dopants "Ductile+" LTS
- Improved performance vs. first gen. ductile materials
- Meeting component level requirements
- 57-58% Bi
- Growing supply base

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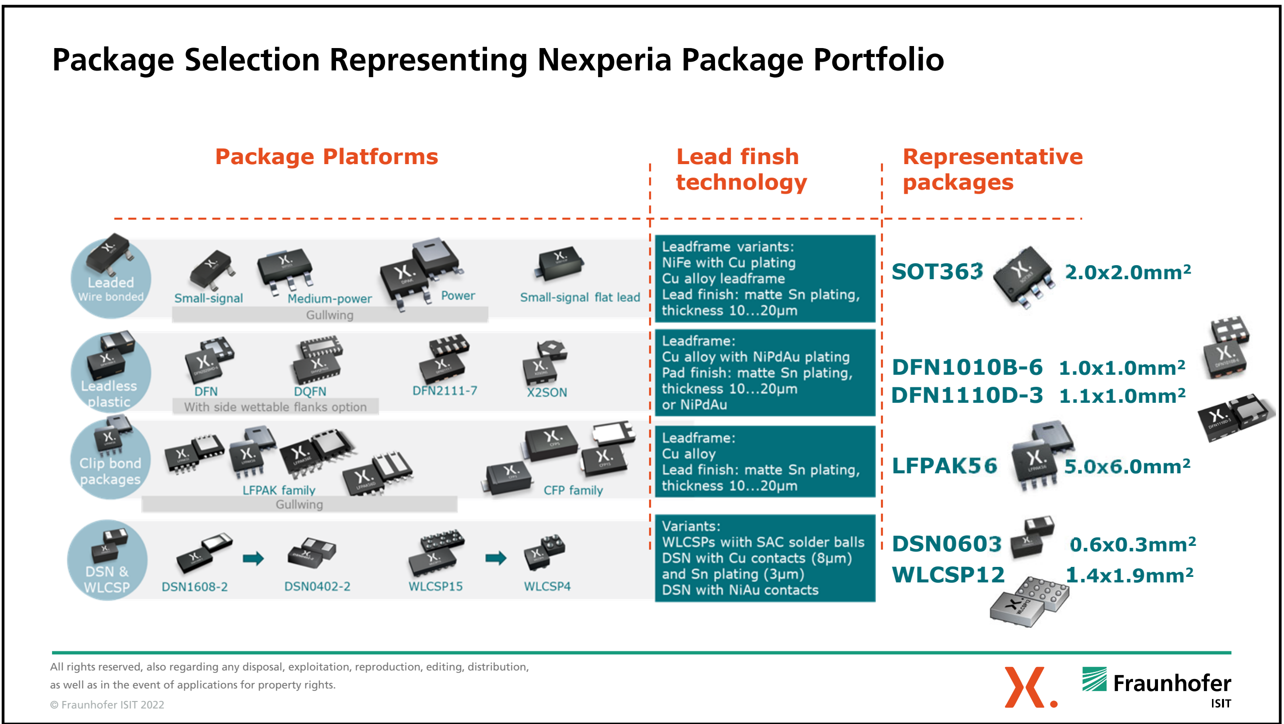

9

Solder Paste Printing

- Solder pastes
  - LTS: SnBiX, Melting point: 138-142°C, ROL0, T4
  - SAC: SAC305, Melting point: 217-219°C, ROL0, T4
- Stencil
  - Stainless steel, brushed, coated, 80µm, 100µm, 120µm

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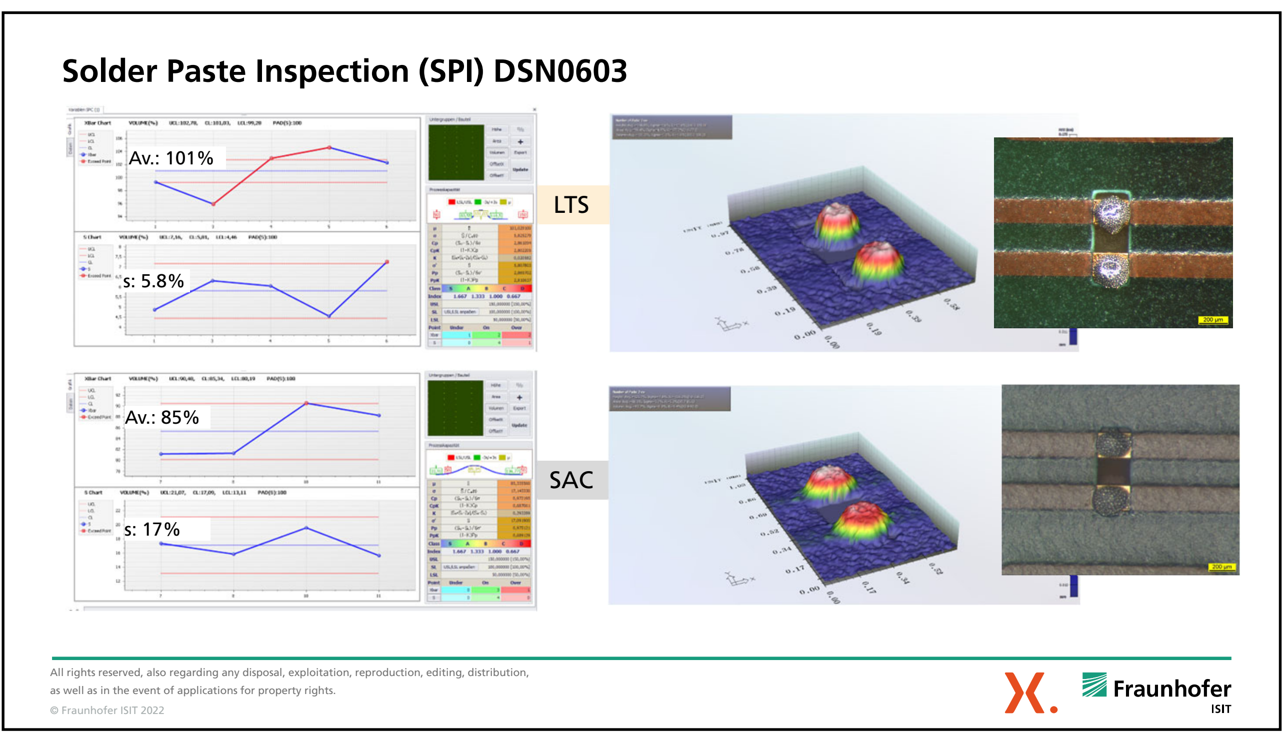
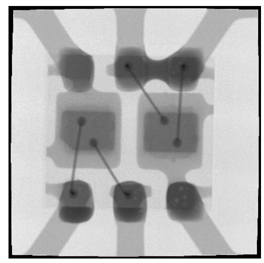


11

Solder Paste Inspection (SPI), summary

Solder paste volume (%)	LTS		SAC		Difference SAC-LTS
Package	Mean value	Deviation	Mean value	Deviation	
DSN0603 (0,6mm x 0,3mm)	101.03	5.82	85.33	17.14	-15.7
DFN1010-6 (1.0mm x 1.1mm)	71.11	14.08	63.36	17.95	-7.75
DFN1110D-3 (1.0mm x 1.1mm)	110.62	25.82	104.61	18.23	-6.01
SOT363 (2.0mm x 2.0mm)	114.47	6.09	108.61	5.31	-5.86
LFPAK56 (6.0mm x 4.9 mm)	101.24	6.85	101.41	6.62	0.17
WLCSP12 (1.36mm x 1.86mm)	93.05	8.79	80.70	11.59	-12.35



DFN1010-6 LTS

Applying LTS paste:

- No solder bridging was found except for DFN1010-6
  - → The limit to get solder bridging for DFN1010-6 is within release ratio of 63-71%
- Observation: small stencil apertures lead to higher amount of solder than using SAC
  - → This is related to the applied flux system and is not LTS specific
  - → For small solder pads an optimization of stencil apertures individual per solder paste is recommended

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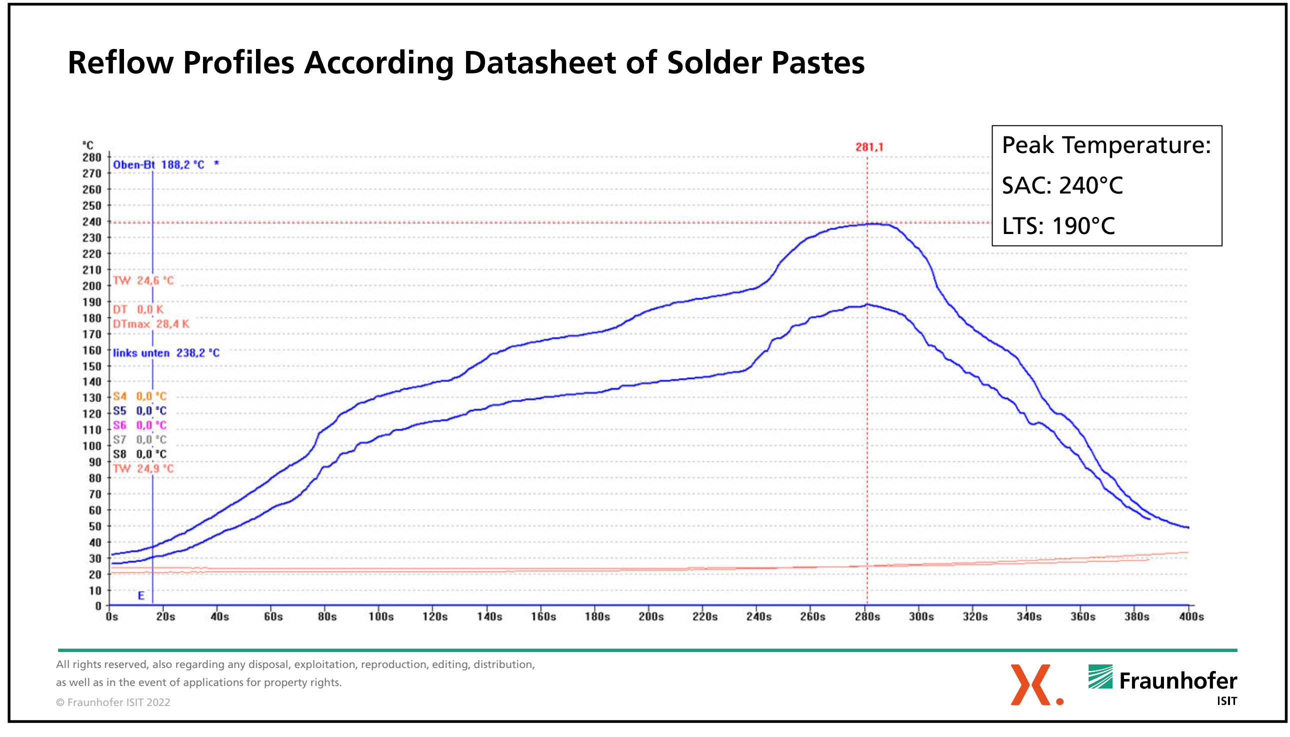
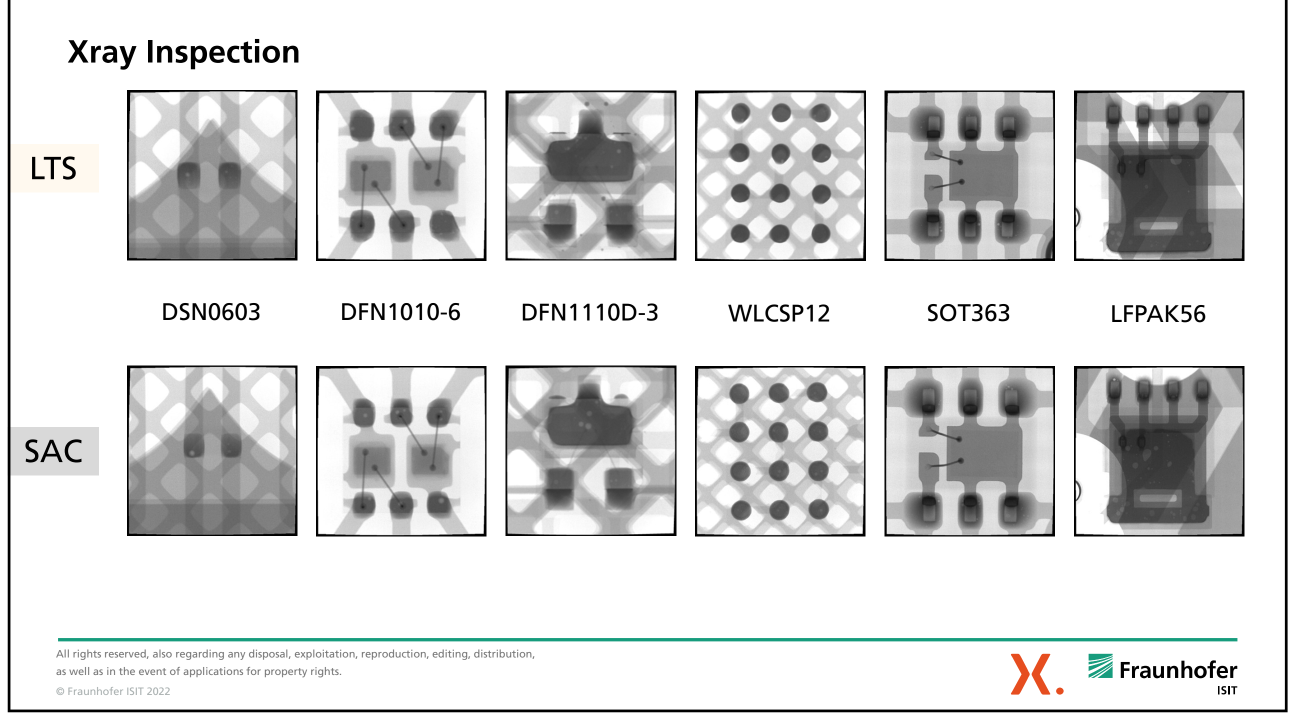
12



13



14

Evaluation of X-Ray analysis

	Voids		Solder Balling		Solder Bridging		Wetting	
Package	LTS	SAC	LTS	SAC	LTS	SAC	LTS	SAC
DSN0603	+	+	+	+	+	+	+	+
DFN1010-6	+	+	+	+	-	+	+	+
DFN1110D-3	+	o	o	+	+	+	+	+
WLCSP12	+	+	+	+	+	+	+	+
SOT363	+	+	+	+	+	+	+	+
LFPAK56	+	o	+	+	+	+	+	+

- Bridging visible on DFN1010-6 using LTS due to high amount of solder paste
  Little solder balling visible on DFN1110D-3 using LTS
  → caused by good release property
- Small uncritical voids visible on DFN1110D-3 using SAC
- Voids visible on LFPAK56 using SAC, uncritical for usual applications

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Tilting and component heigth of BTC and WLCSP12

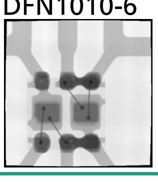
Solder	LTS				SAC			
	Max. Tilting angle		Max. height difference	Mean height	Max. Tilting angle		Max. height difference	Mean height
Package	long side	short side			long side	short side		
DSN0603	0.6	15.2	77	336	2.2	15.3	70	336
DFN1010-6	2.8	0.4	56	358*	0.7	2.2	42	385*
DFN1110D-3	0.4	4.6	61	505	0.3	4.1	65	505
WLCSP12	0.5	0.8	19	556**	0.3	0.2	26	532**

No significant difference between LTS and SAC, except:

* Difference due to solder volume (bridging) with LTS

** Difference due to incomplete melting of SAC ball

DFN1010-6



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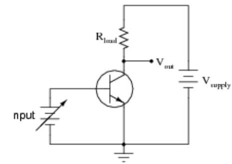
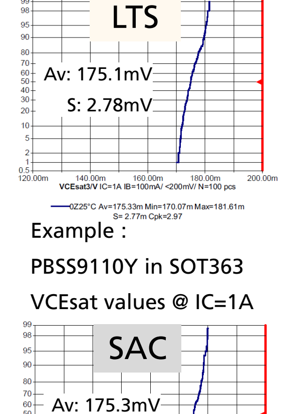
Electrical Test Results, after soldering

- Electrical testing after soldering the devices on PCB was done with the standard test jobs per type
- No solder related differences could be detected between devices soldered with SAC and LTS
- Exceptions are the shorts caused by solder bridges of DFN1010-6 devices

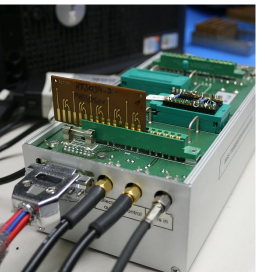




Example :

PBSS9110Y in SOT363

VCEsat values @ IC=1A



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17

Electrical Test Results after TCT -40°C/+85°C

-40°C/+85°C	DSN0603-2		DFN1010B-6		SOT363		LFPAK56	
	LTS	SAC	LTS	SAC	LTS	SAC	LTS	SAC
0 c	0/100	0/100	12/100 **)	0/100	0/100	0/100	0/100	0/100
500 c	0/100	0/100	0/88	0/100	0/100	0/100	0/100	0/100
1000 c	0/95	0/95	0/83	0/95	0/95	0/95	0/95	0/95
1250 c	0/90	0/90	0/78	0/90	0/90	0/90	0/90	0/90
1500 c	0/85	0/78*)	0/73	0/85	0/85	0/85	0/85	0/85

Remarks:

One PCB was taken out after 500c, 1000c,1250c, 1500c for mechanical analysis

*) Some parts were mechanically damaged, this explains the reduced amount at 1500c

**) solder bridges due to better paste print release performance caused these failures

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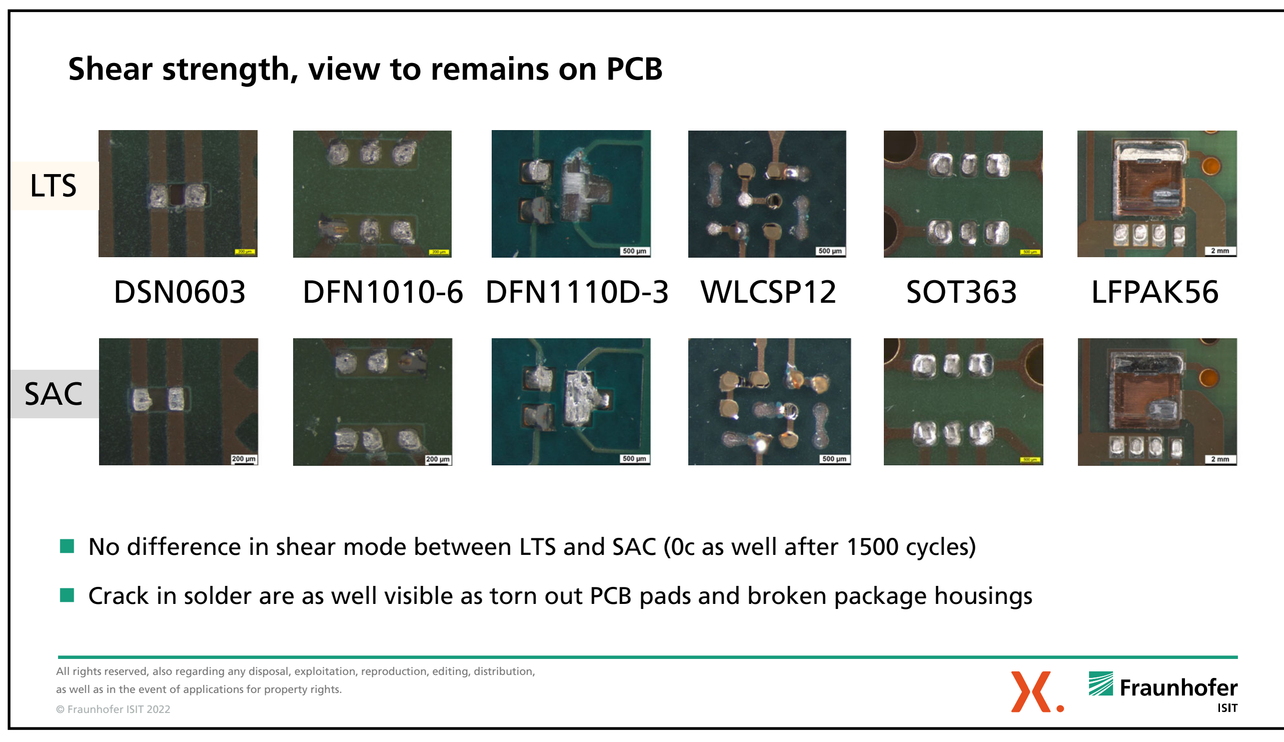

19

Shear strength comparison, TCT -40°C/+85°C , 0c vs 1500c

Package	Shear Strength [N/mm²]				Shear Mode
	0 cycles		1500 cycles		
	LTS	SAC	LTS	SAC	
DSN0603	73.37	68.87	61.29	60.82	Solder joint
DFN1010-6	77.12	72.37	76.08	65.06	Solder joint / Package
DFN1110D-3	42.51	36.57	40.67	34.05	Solder joint / Package / PCB
WLCSP12	30.16	32.52	32.48	31.21	Package / PCB
SOT363	44.08	29.27	36.43	28.33	Solder joint
LFPAK56	18.35	14.36	17.53	15.04	Package

- Shear strength fulfill industry established limit of 20N/mm², even after TCT, except LFPAK56
- For LFPAK56 shear mode is package breakage due to large heatsink which result in very solid solder connection: shear force values ~30Kg which confirms package and solder joint is very robust for applications
- Acceptable shear strength degradation after TCT, except WLCSP12 (value is within spread of measurement)
- Shear strength is higher using LTS, because of higher mechanical material strength

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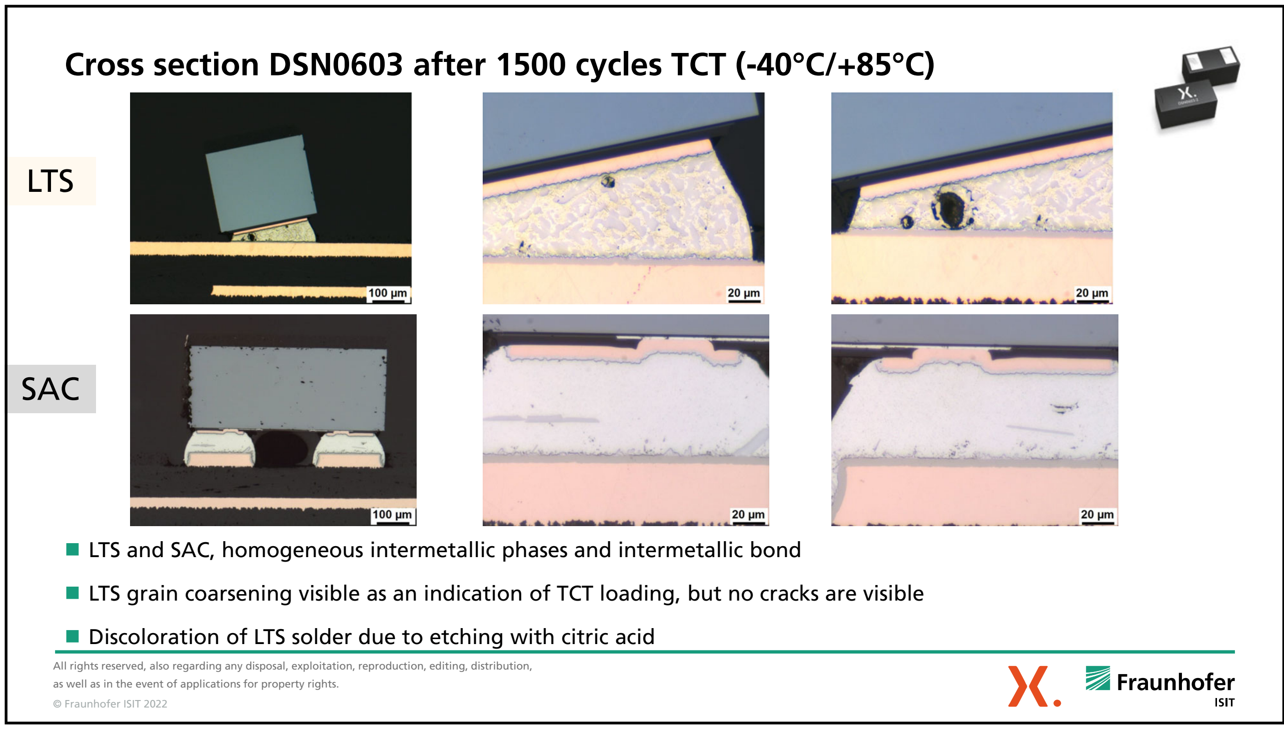
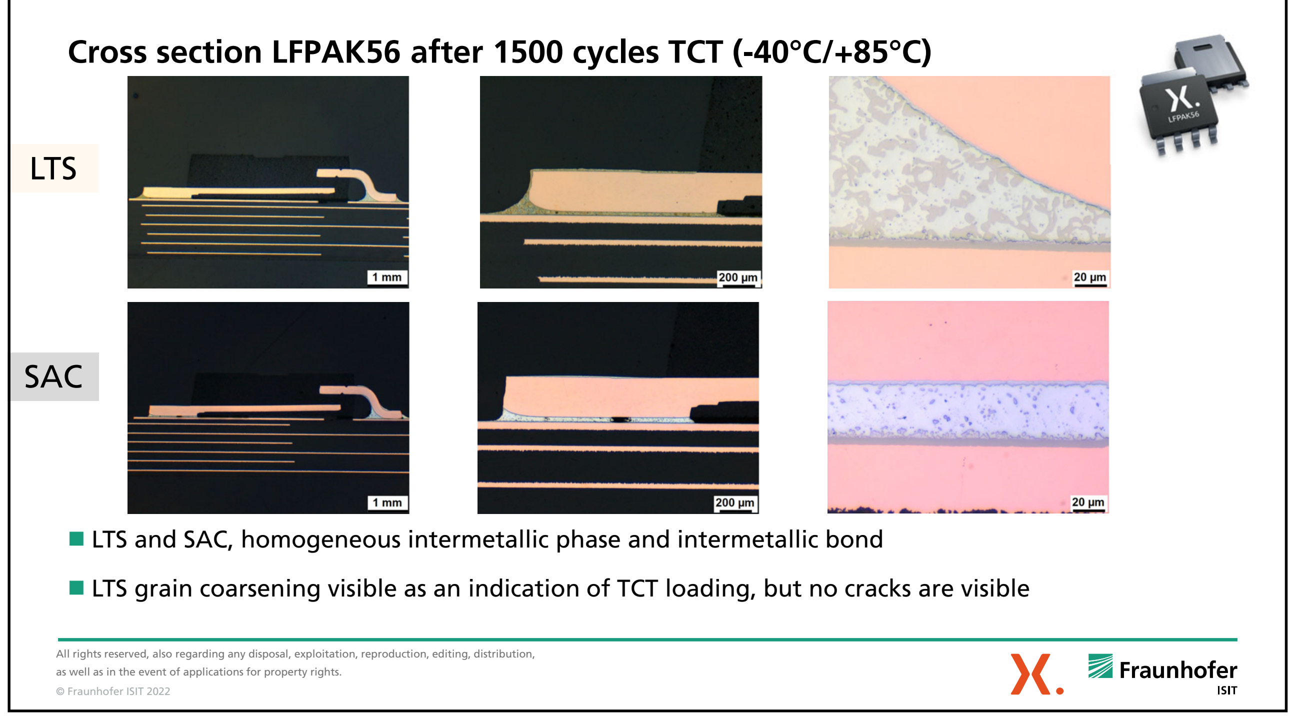


21



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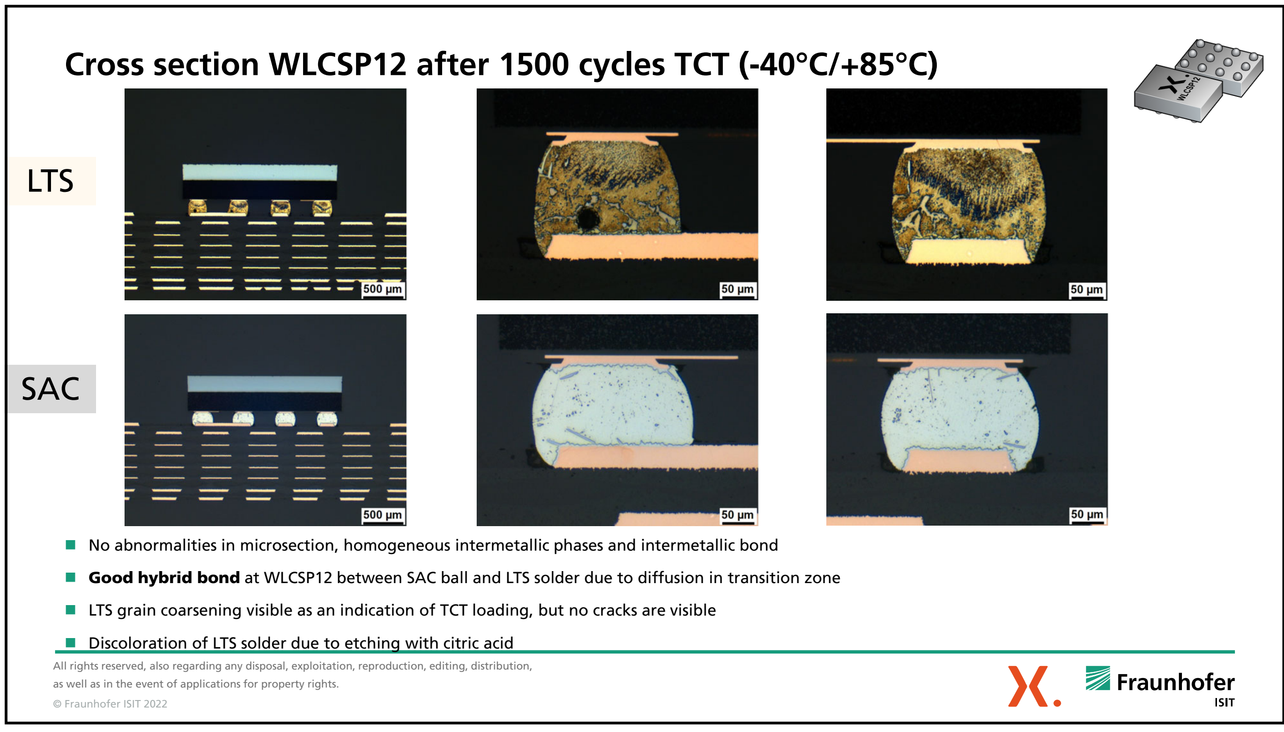
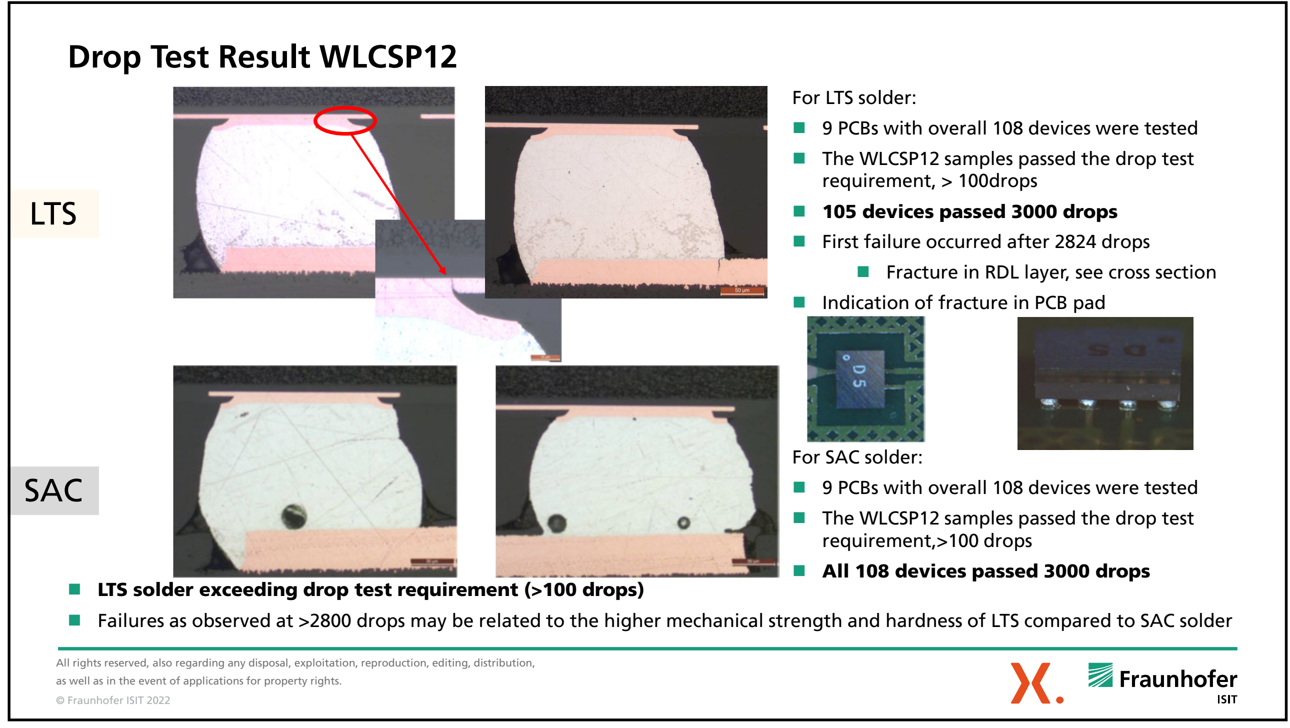


23



24

Summary of Present Results

- **Component wetting** according to ceramic plate test **is equally good** with SAC and LTS
- Solder bridging occurs with DFN1010-6 using LTS (stencil apertures should be optimized)
- **No abnormalities in cross section**: Good wetting of both solder pastes, homogeneous intermetallic phases and bond
- **Good hybrid bond** for WLCSP12 between SAC balls and LTS solder due to diffusion in transition zone
- Shear strength is higher using LTS
- No difference in electrical performance measurable
- Microsections after 1500 cycles -40°C/+85°C
  - Homogeneous intermetallic phases and intermetallic bond, no cracks observed using LTS solder
  - LTS grain coarsening visible as an indication of TCT loading, but no cracks are visible
- **All investigated packages show good reliability using SnBiX or SAC solder pastes**

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Herausforderung

- Prozesssichere Verarbeitung sicherstellen: Handling, Oberflächen der Fügepartner, Lötprozessfenster
- Grenzen des „Mission Profile“ (Temperaturbelastbarkeit) definieren/ausloten
- Grenzflächenreaktionen verstehen
- Prüfstandards zur Qualifizierung von Niedertemperatur-Weichlötprozessen derzeit ungeeignet

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Ausblick

- diverse bilaterale Entwicklungsprojekte

Forschungsprojekt in der Antragsphase

- „Zuverlässigkeit niedrigschmelzender Weichlote auf SnBiX-Basis in der Elektronikfertigung mit ganzheitlicher Lötbarkeitsbetrachtung unter Berücksichtigung von Wirkmechanismen an den Grenzflächen“

Forschungsziel

- Definition des Prozessfensters (speziell untere Grenztemperaturen) für einen prozesssicheren Niedertemperaturweichlötprozesses zur Herstellung zuverlässiger Elektronik
- Vertieftes Verständnis über bisher wenig erforschte Grenzflächenreaktionen beim Niedertemperaturweichlöten und deren Phasenwachstum/ Kornvergröberung nach beschleunigter Alterung (Zuverlässigkeitsergebnisse)
- Energiebetrachtung, Ressourcenschonung, Technikfolgenabschätzung
- Erweiterung von Prüfstandards zur Qualifizierung von Niedertemperatur-Weichlötprozessen

27

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