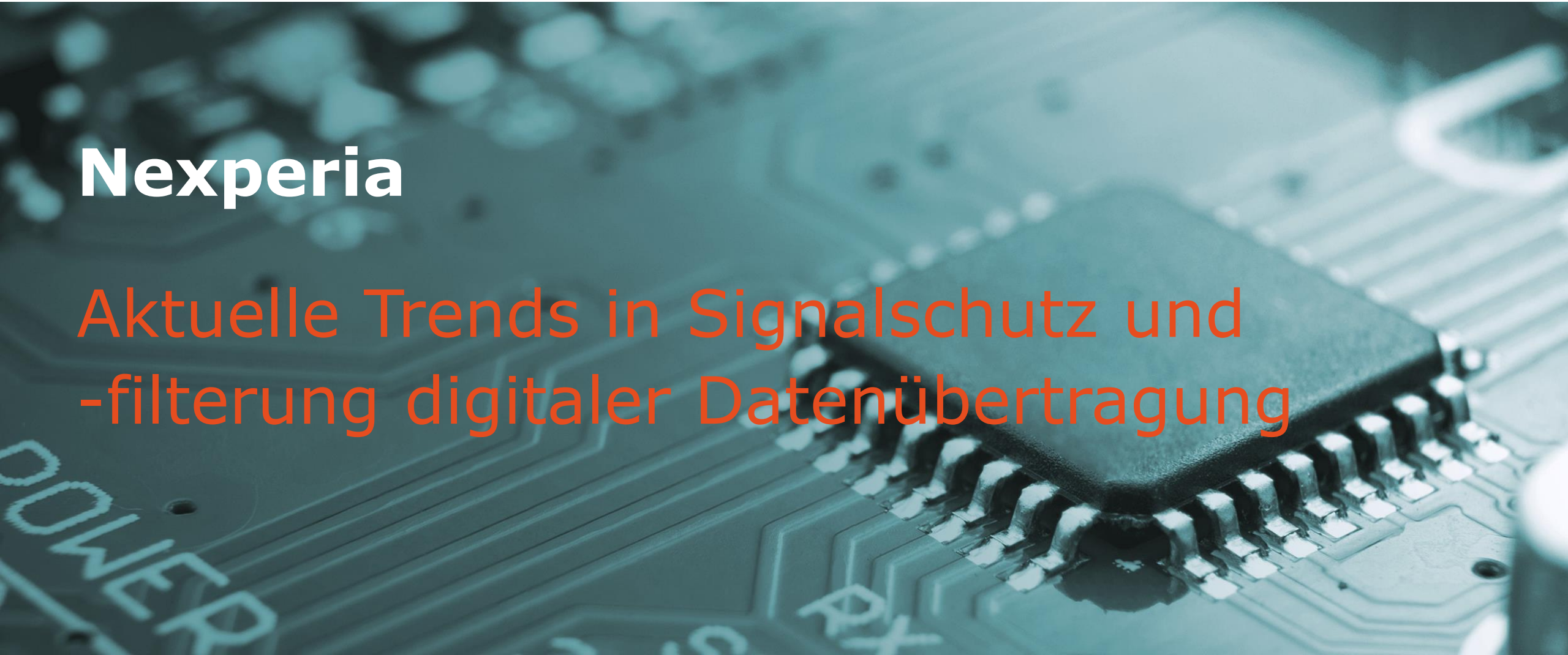
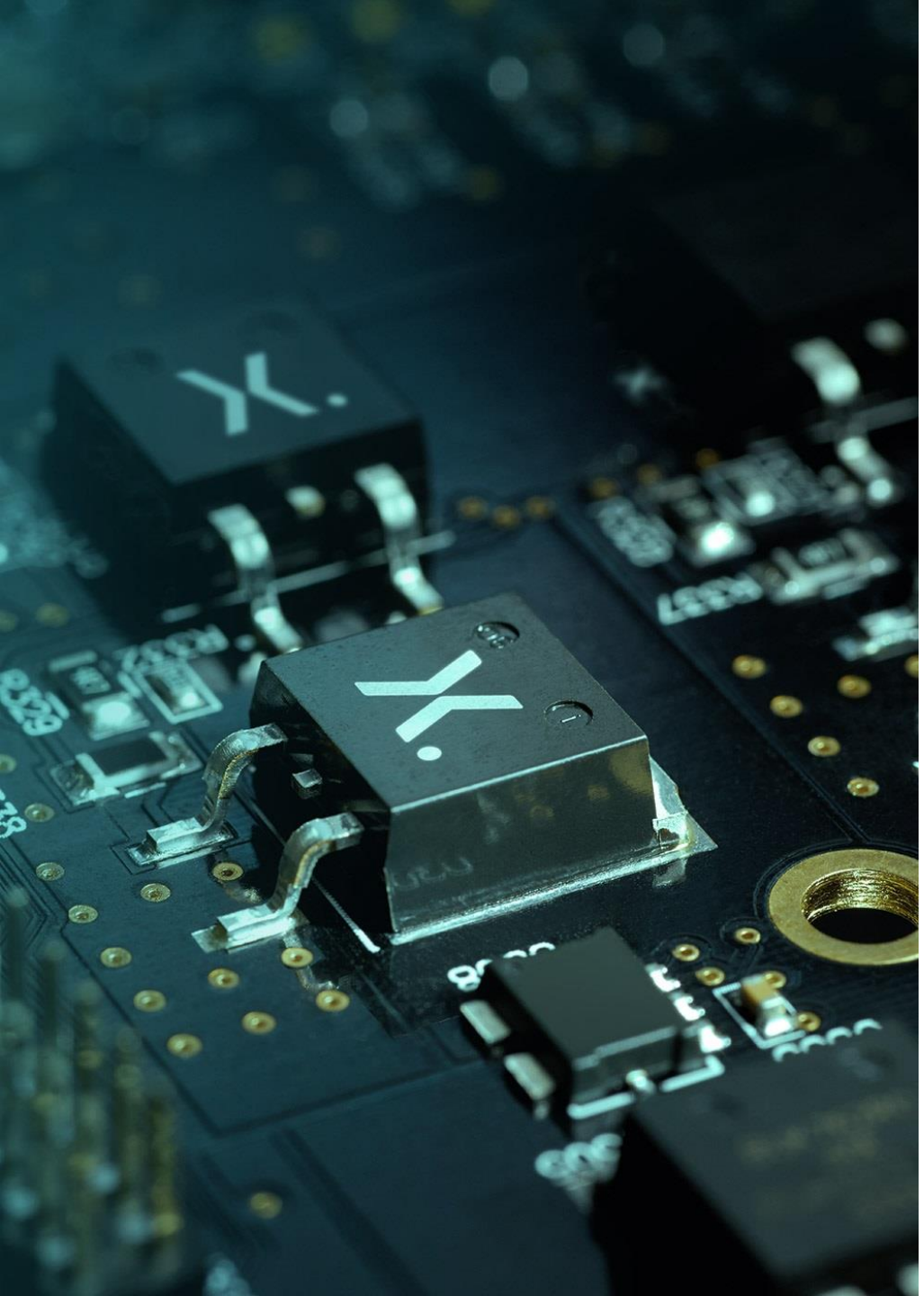
Burkhard Laue, Application Marketing
13. September 2018



Nexperia

Aktuelle Trends in Signalschutz und -filterung digitaler Datenübertragung

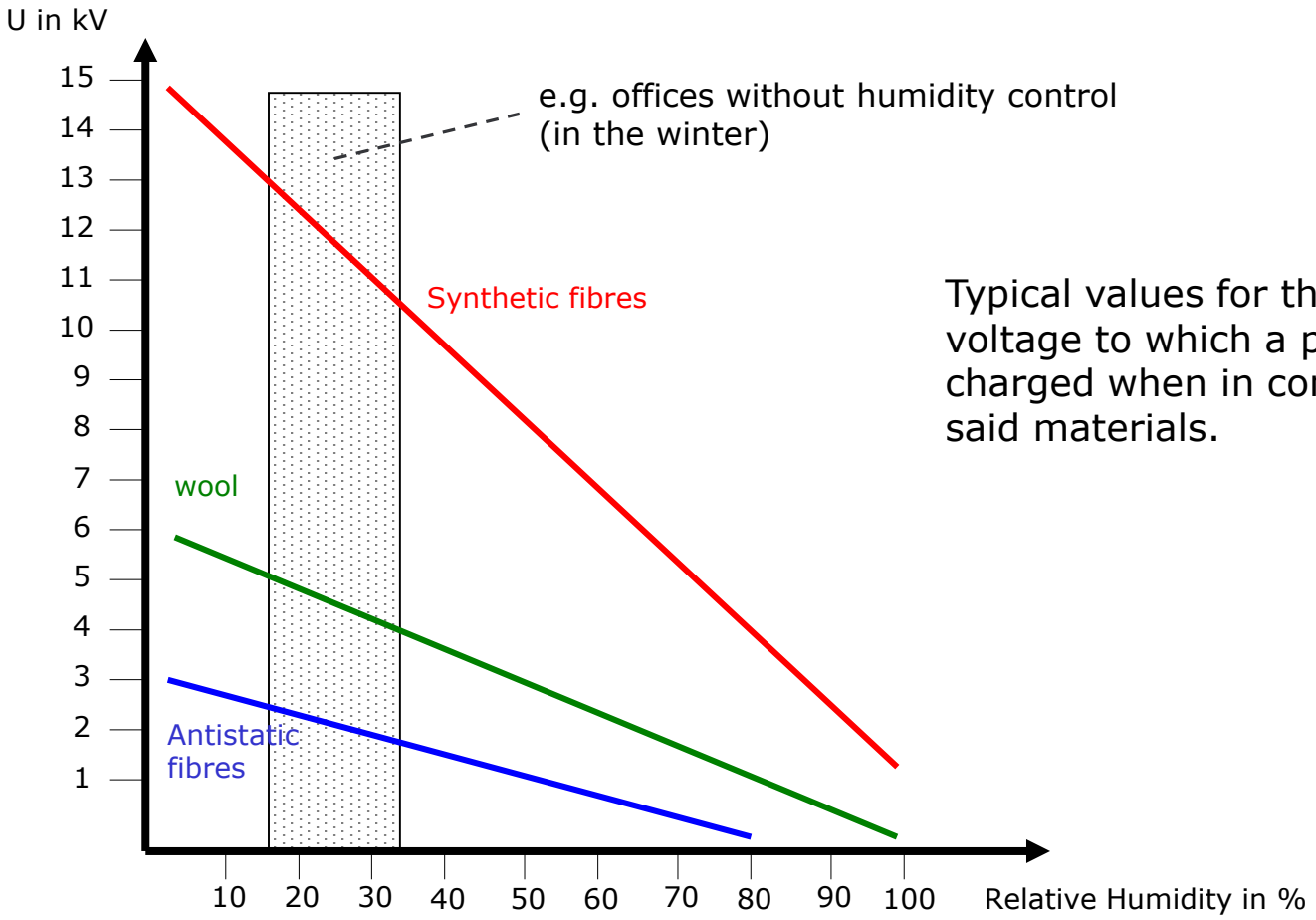


Agenda

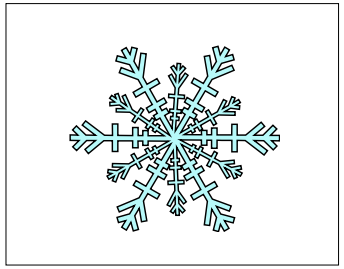
- General aspects for ESD
- Testing methods - IEC61000, TLP, VF-TLP..
- ESD protection selection criteria for ESD protection, latest findings for super speed interfaces
- Topology of snap-back ESD protection devices
- Common Mode Filters with ESD protection

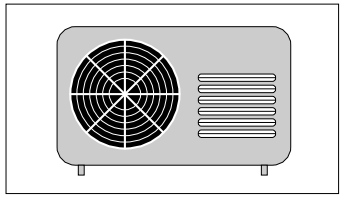
ESD – Electro Static Discharge

Material / environmental influences affect charge separation



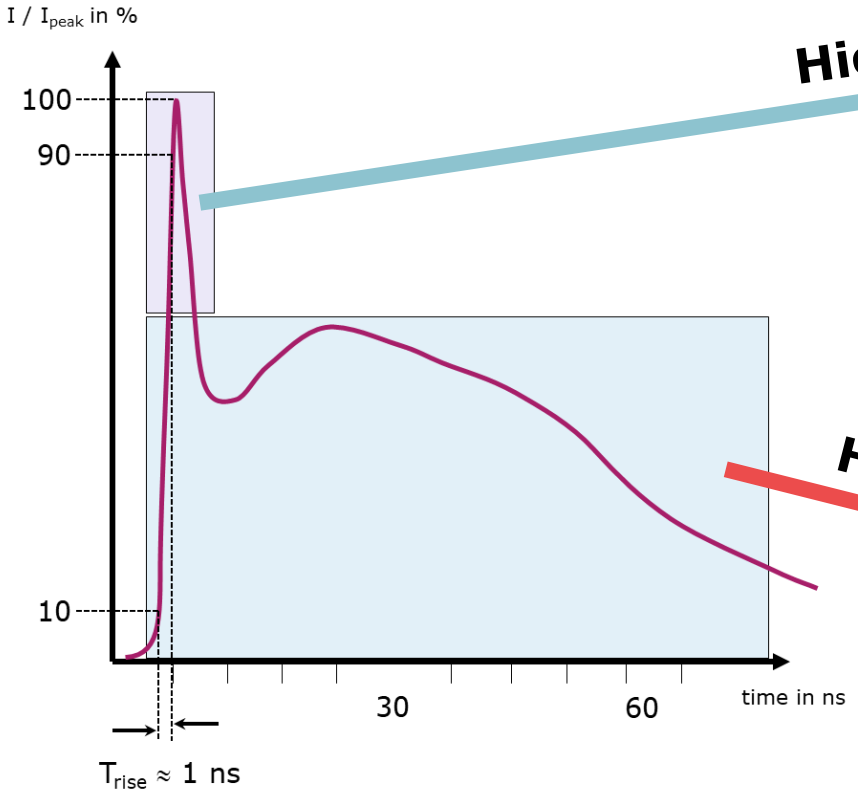
Typical values for the electrostatic voltage to which a person can be charged when in contact with said materials.





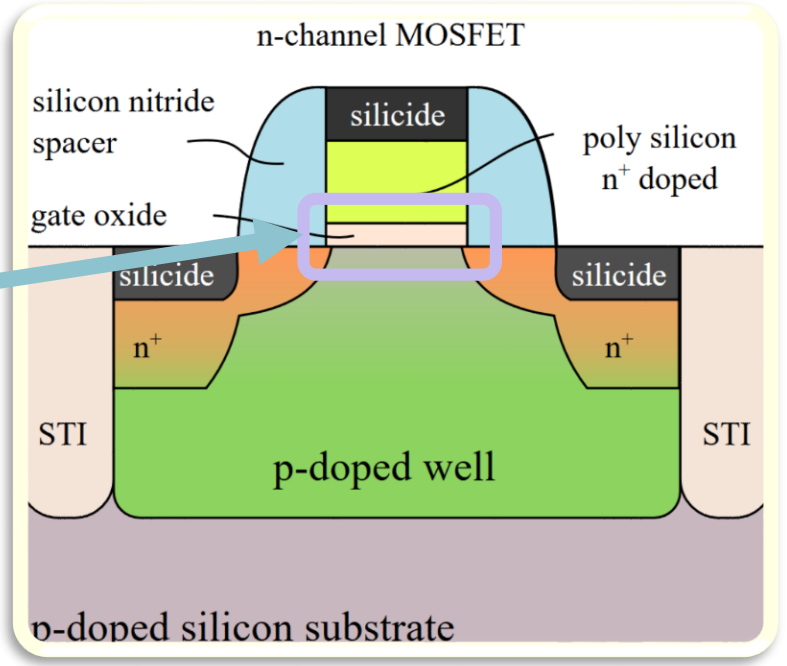
ESD – Defects caused by ESD

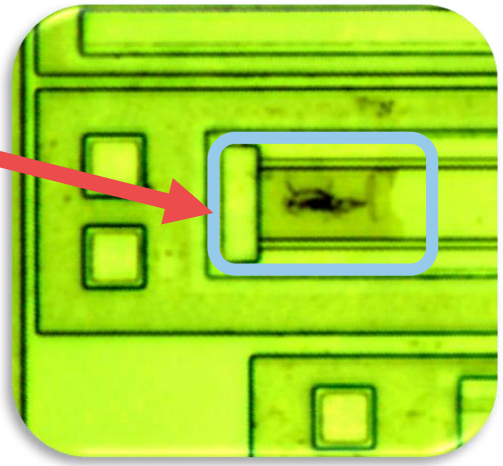
Destruction mechanism



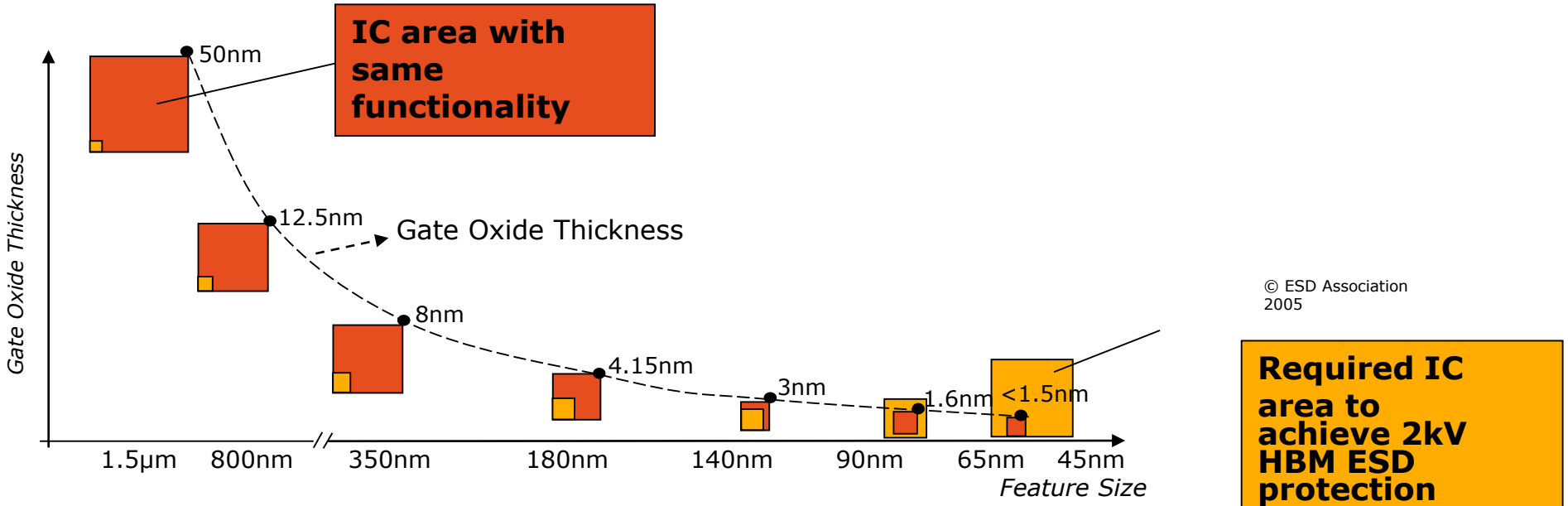
High voltage

High energy





ESD Damage – IC technology trend



- Trend: Chip size decreases to a minimum
  - Gate thickness and chip size (channel length) decreases
  - Maximum gate voltage decreases (e.g. for CMOS090 <1.5V static)
  - New Processes are optimized for area and performance, *NOT for ESD performance!*
- Impact: Modern ICs designs are very sensitive to ESD strikes
  - ICs failure due to gate oxide punch through from high voltages
  - ICs failure from Joule heating due to high residual currents

  → *Additional board level ESD protection for external interfaces becomes a must!*

Super speed interfaces

Data Speed Increase

Table 7: Overview of data rates for USB interfaces

USB Type	Speed class	Data Rate	Symbol rate (Baud rate) Coding method
USB 1.0	Low Speed (LS)	1.5 Mbit/s = 187.5 kByte/s	1.5 MByte/s NRZI-Code with Bit-Stuffing
USB 1.0	Full Speed (FS)	12 Mbit/s = 1.5 Mbit/s	12 Mbit/s NRZI-Code with Bit-Stuffing
USB 2.0	High Speed (HS)	480 Mbit/s = 60 MByte/s	480 Mbit/s NRZI-Code with Bit-Stuffing
USB 3.0	Super Speed	4000 Mbit/s = 500 MByte/s	5000 Mbit/s 8b10b-Code
USB 3.1	Super Speed +	9697 Mbit/s = 1212 MByte/s	10000 Mbit/s 128b132b-Code
USB 3.2	Super Speed +	2 lane operation with Type-C connector operation; doubling of effective data rate	

Table 22: List of HDMI key parameters f

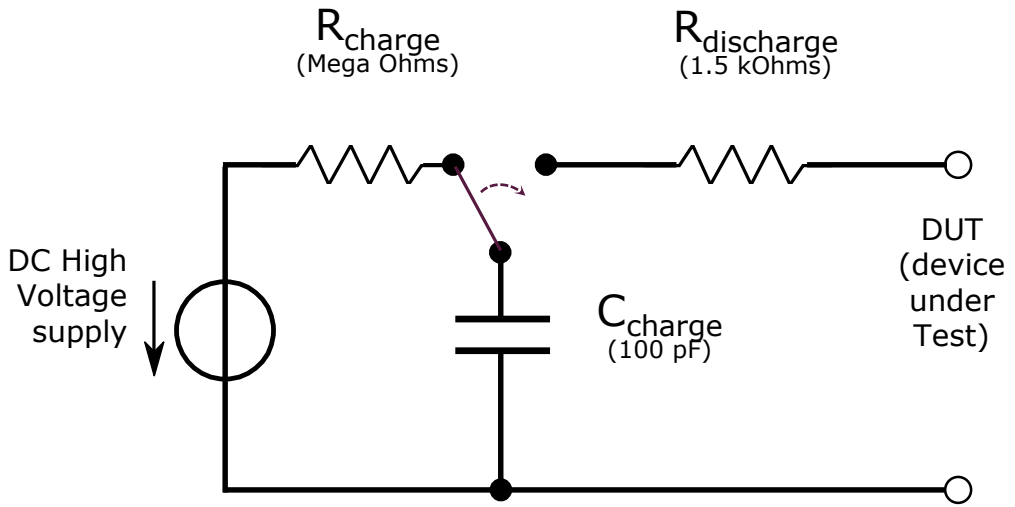
HDMI version	1.0	1.1	1.2	1.3	1.4	2.0	2.1
Maximum pixel clock rate (MHz)	165	165	165	340	340	600	no extra clock channel
Maximum TMDS bit rate per lane including 8b/10b coding overhead (Gbit/s)	1.65	1.65	1.65	3.4	3.4	6	12
Maximum total TMDS throughput including 8B/10b coding overhead (Gbit/s)	4.95	4.95	4.95	10.2	10.2	18	48
Maximum audio throughput bit rate (Mbit/s)	36.86	36.86	36.86	36.86	36.86	49.152	49.152
Maximum video resolution over 24 bit/pixel single link	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60 Hz	1920* 1200 p/ 60Hz	2560* 1600 p/ 60 Hz	4096* 2160 p/ 30 Hz	4096* 2160 p/ 60 Hz	7680* 4320 p/ 60 Hz
Maximum color depth (bit/pixel)	24	24	24	48	48	48	48

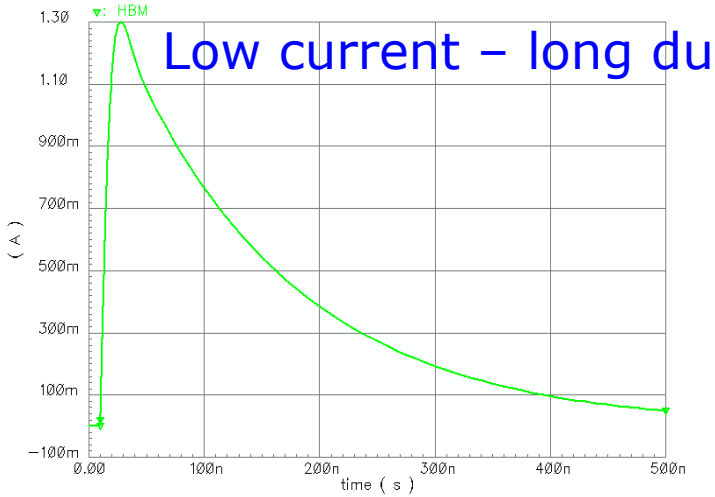
Testing methods

ESD – Device Level Testing: HBM

Human Body Model

- HBM was developed to simulate the discharge of a human body to a grounded device (IC).
- To replicate an RC network is used:
  - $R_{discharge}$ = 1500 ohms
  - C = 100 pF
- ANSI / ESDA / JEDEC JS-001-2012 for Semiconductor Components
- **Different** from standard EN 61000-4-2 for devices (system level test)



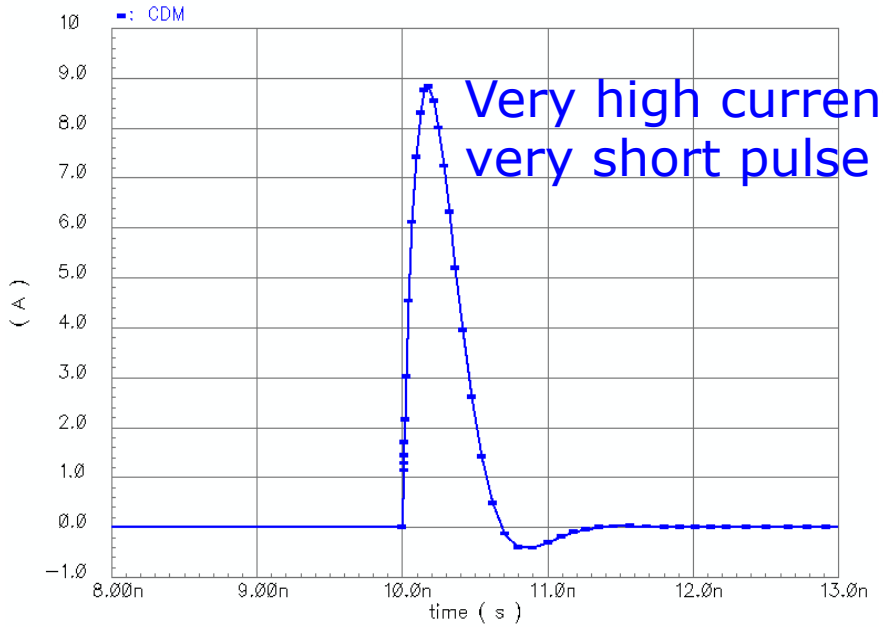


Low current – long duration

ESD – Device Level Testing: CDM

Charged Device Model

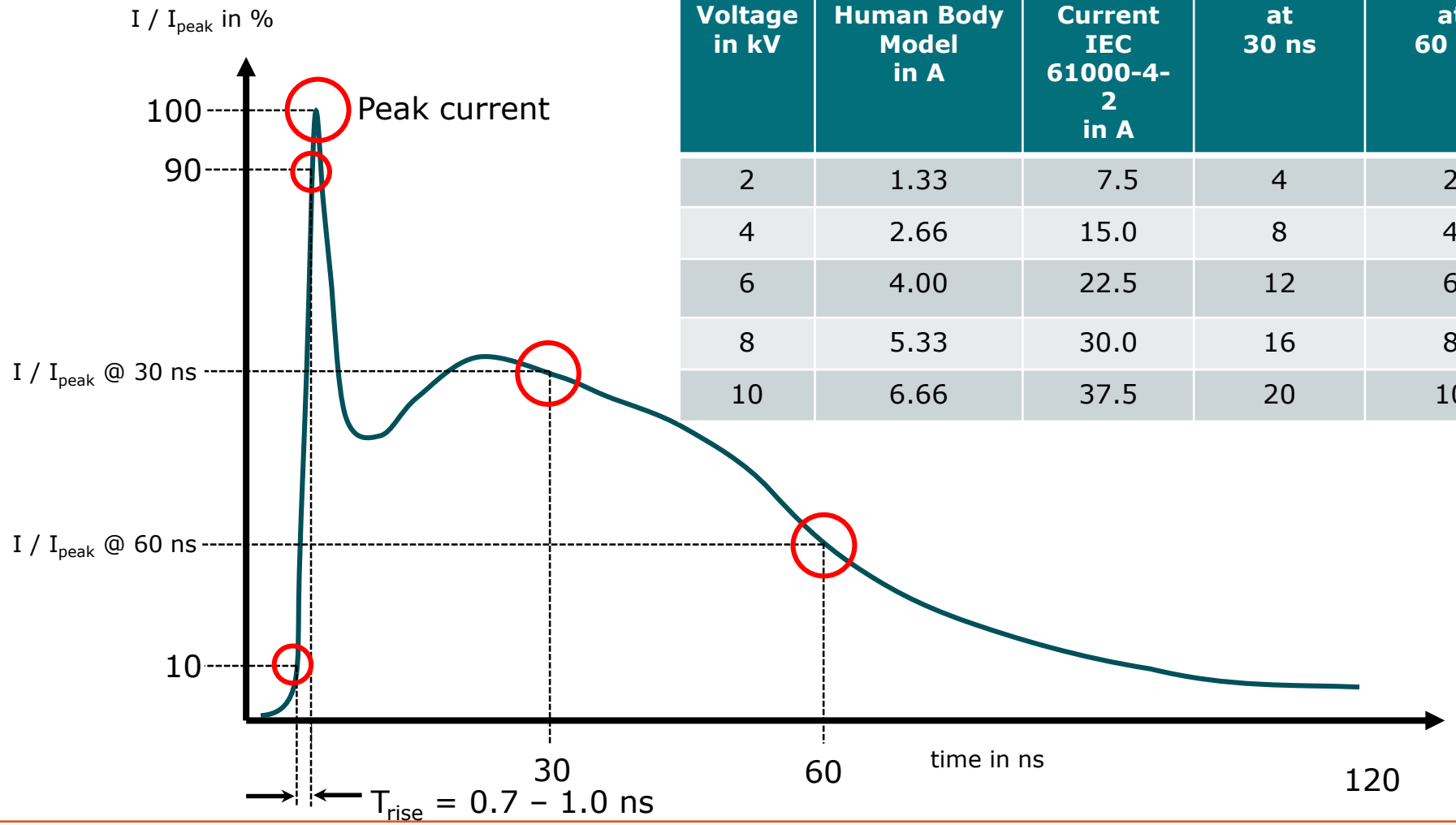
- CDM emulates the process of charging / discharging that can occur in production environments.
- For example, ICs that are poured from plastic tubes and hit a metallic surface.
- It is conceivable that charges have accumulated on the metal pins of an IC or on the package, ultimately discharging through a single grounded pin.
- The discharge current is limited only by parasitic impedances and capacitance.



ESD – System Level Testing: IEC 61000-4-2

Typical waveform of ESD current

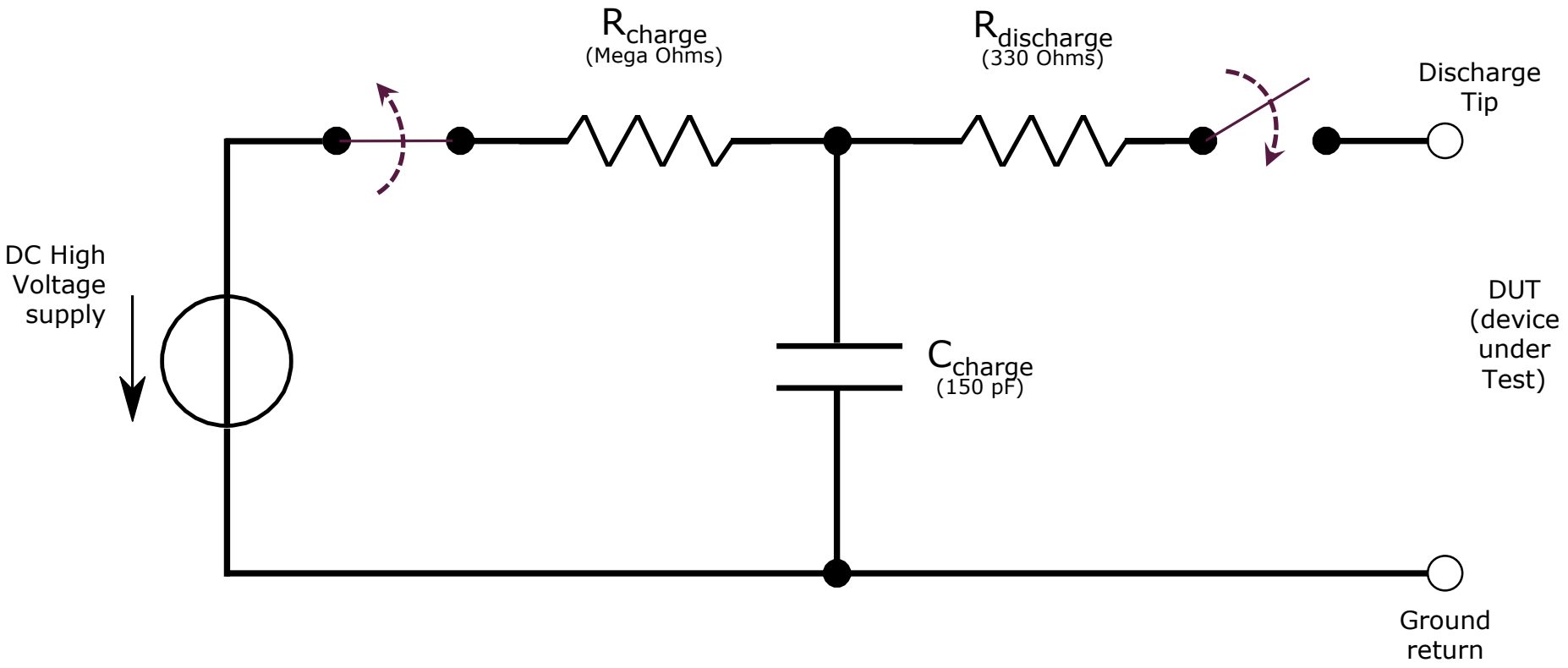
- Rise time
  - 0.7 – 1 ns
    (von 10% auf 90%)
- Peak current
  - +/- 10% tolerance
- Current after 30 ns
  - +/- 30% tolerance
- Current after 60 ns
  - +/- 30% tolerance



Applied Voltage in kV	Peak Current Human Body Model in A	Peak Current IEC 61000-4-2 in A	Current at 30 ns	Current at 60 ns
2	1.33	7.5	4	2
4	2.66	15.0	8	4
6	4.00	22.5	12	6
8	5.33	30.0	16	8
10	6.66	37.5	20	10

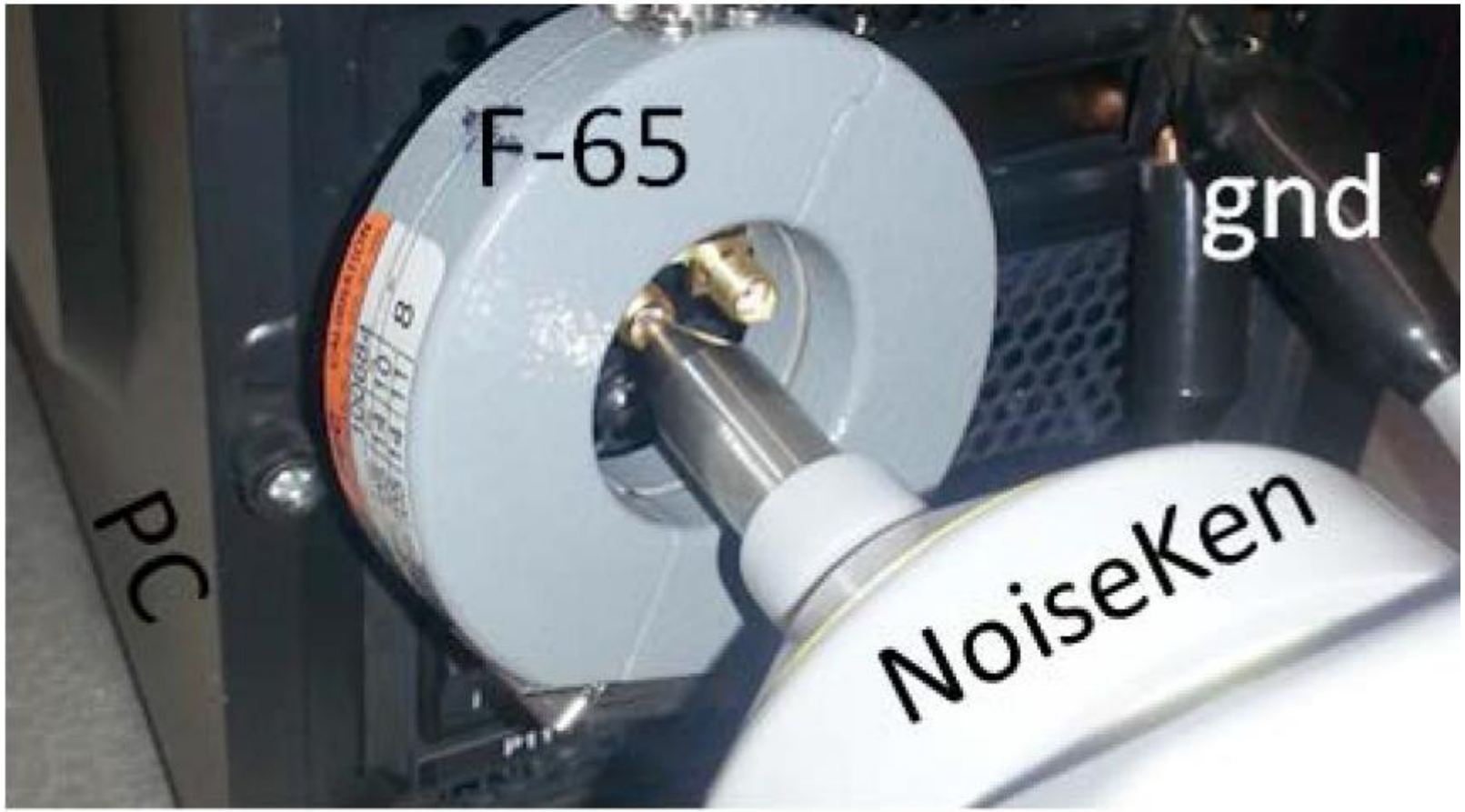
ESD – System Level Testing: IEC 61000-4-2

Simplified equivalent circuit diagram of ESD test generator



ESD pulse waveform variation (1)

NoiseKen gun monitored with F-65 current probe



ESD pulse waveform variation (2)

NoiseKen gun monitored with F-65 current probe, shots on 2 Ohm Pellegrini target

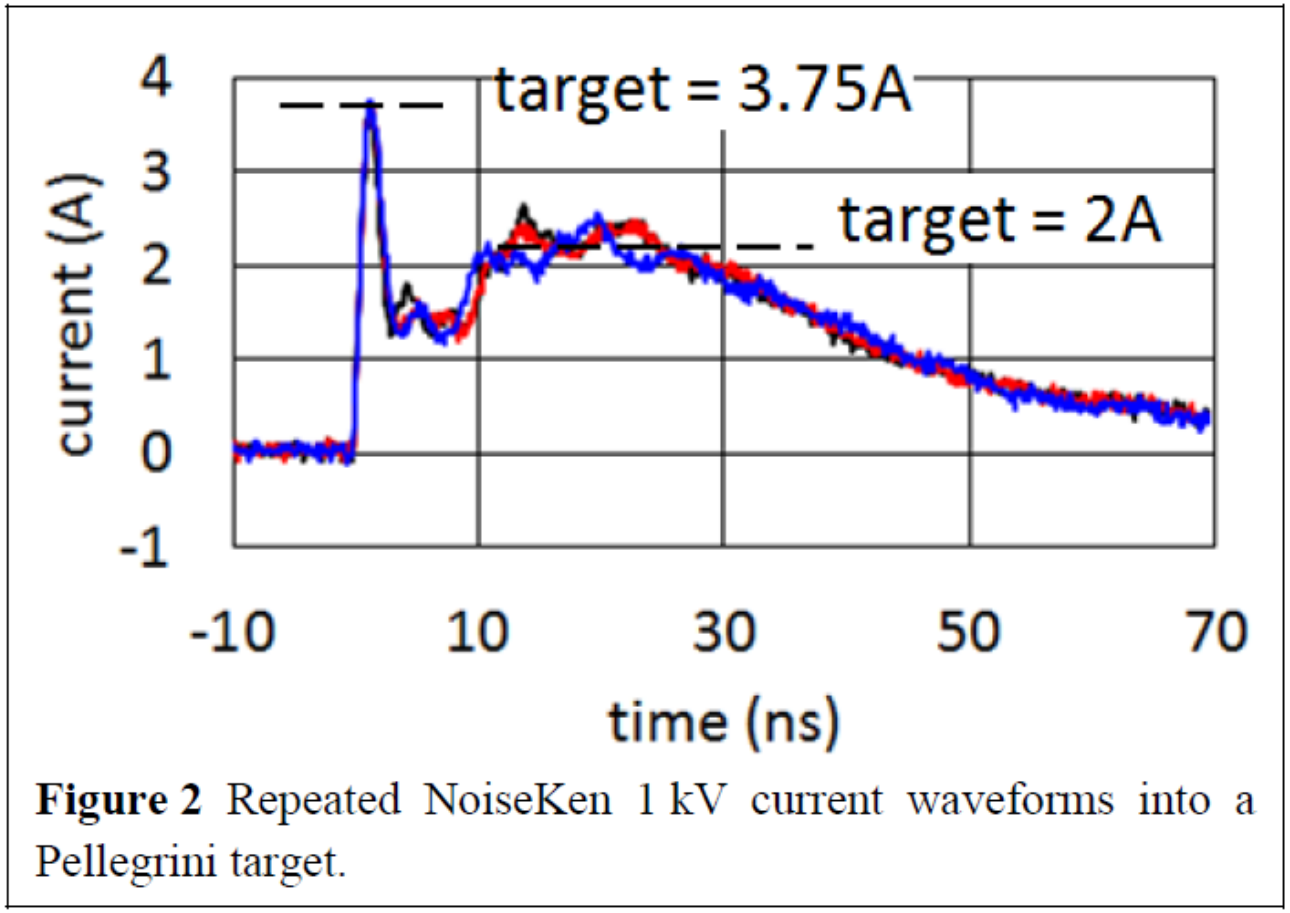


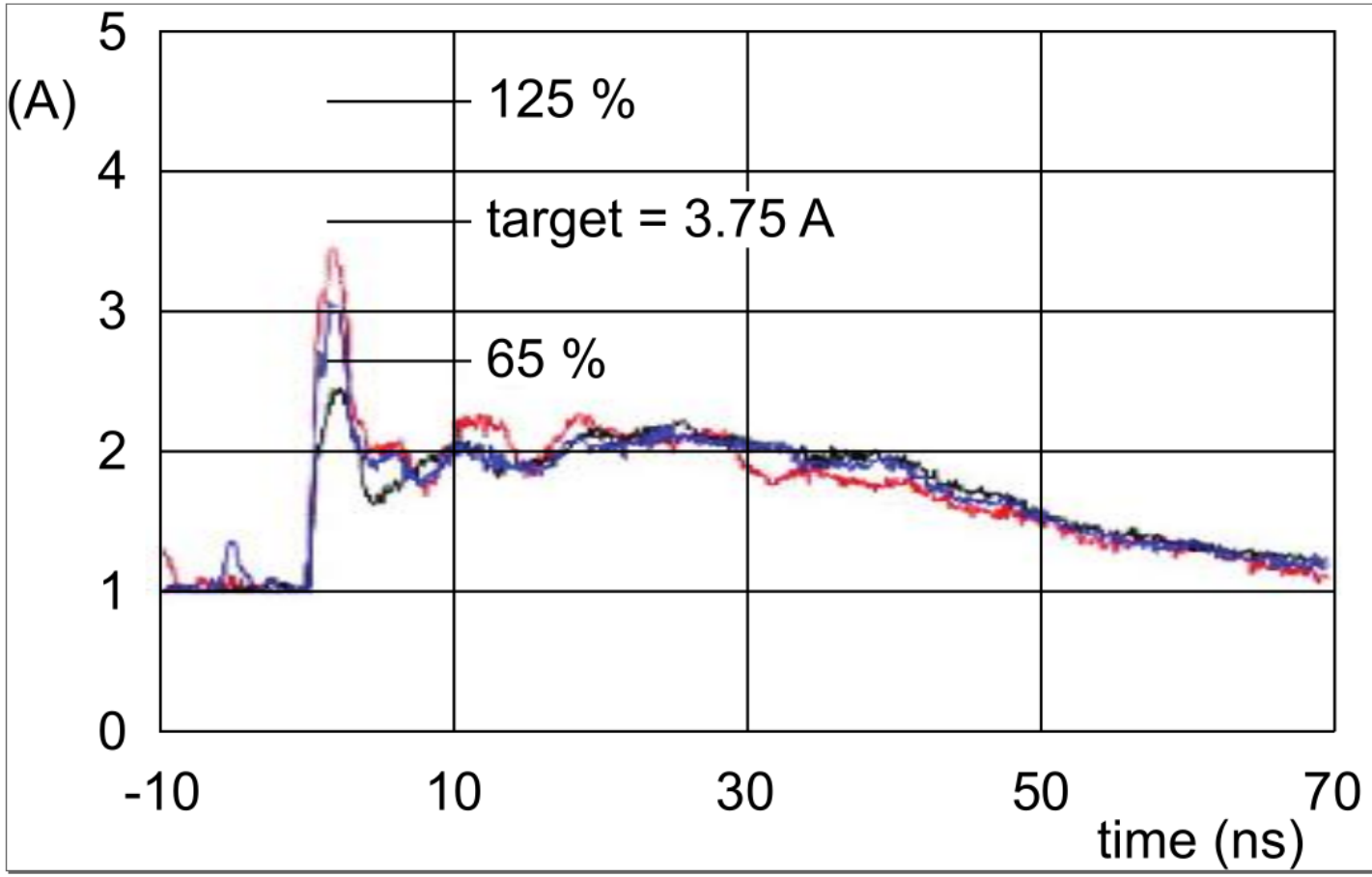
Figure 2 Repeated NoiseKen 1 kV current waveforms into a Pellegrini target.

Waveforms compliant
To IEC61000-4-2,

Good reproducibility

ESD pulse waveform variation (3)

NoiseKen gun monitored with F-65 current probe, shots at PC system target



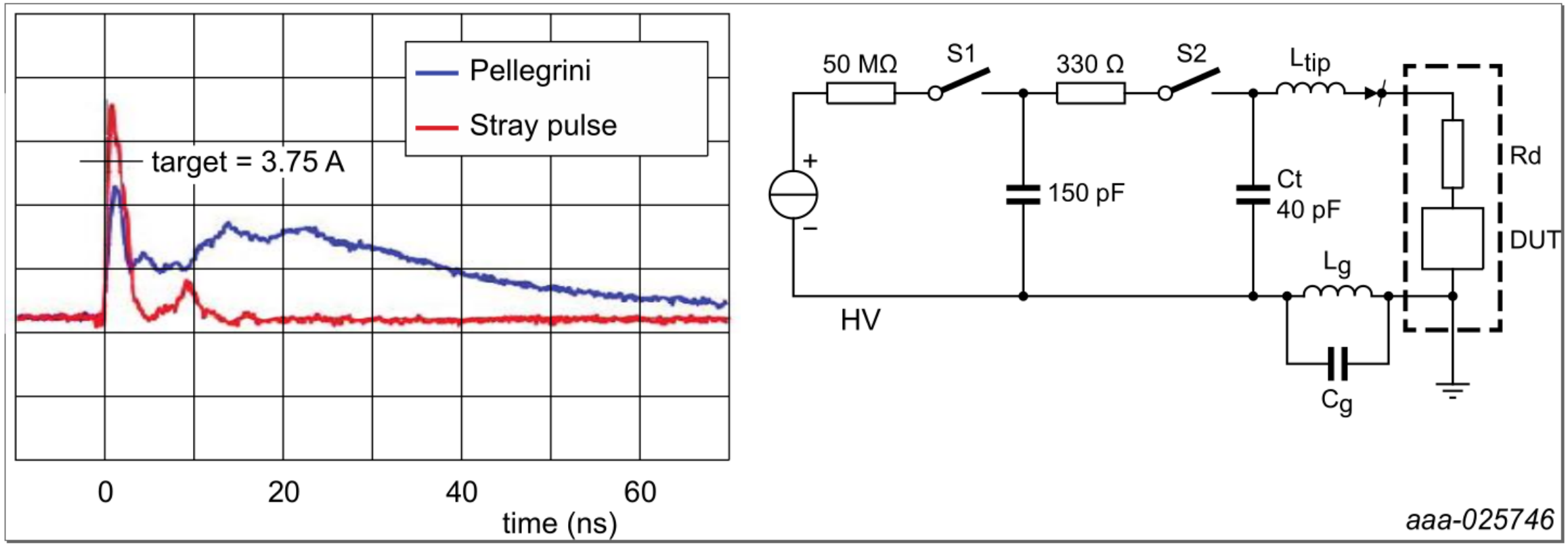
reference is IEC 61000-4-2
1st peak 3.75 A ± 15 %
2nd peak 2A ± 30 %

2nd peak stable and in spec
1st peak -35 % to +25 % variation
out of specification

aaa-025744

ESD stray pulses

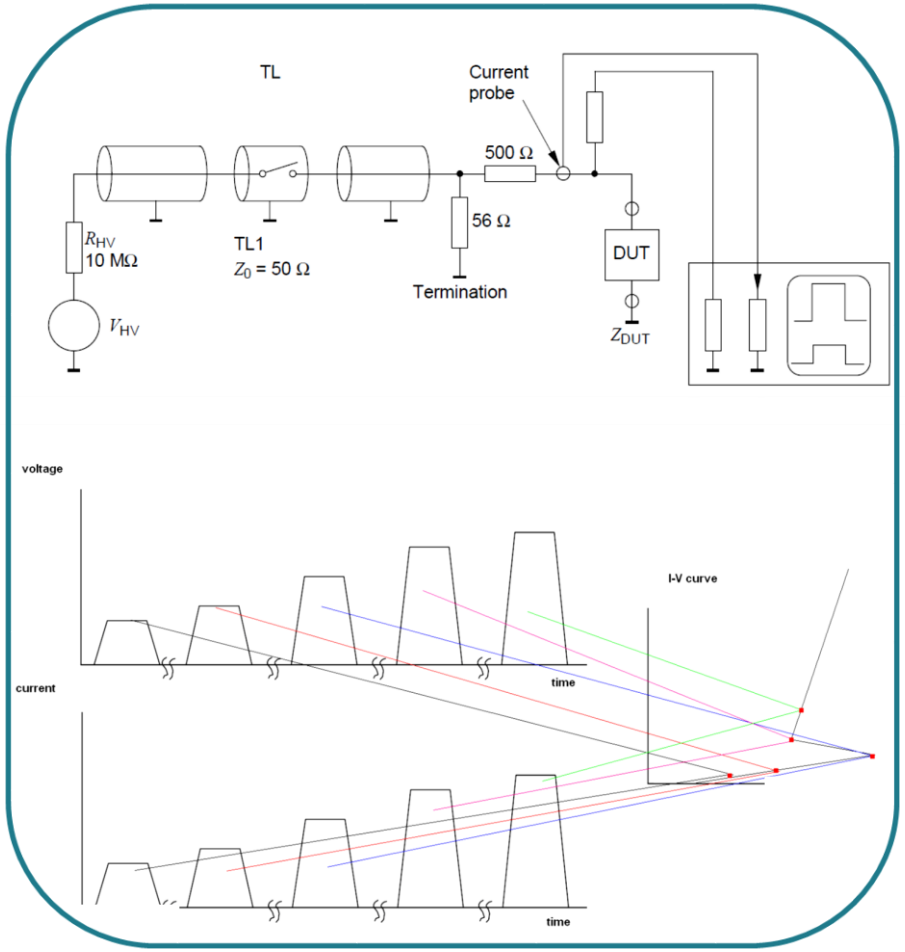
Nexperia recommends to short the gun to GND before contacting the target, the remove the ground connection and start to shoot.



TLP measurement (1)

Principle of TLP Measurement

- Device under Test (DUT) is subjected to rectangular current pulses
- Duration of these pulses is between 5ns – 100 ns,
- The current is increased step by step, until the system starts to show a failure
- Connecting the results to an I_{DUT} versus V_{DUT} curve describes the response of a system for ESD surge events
- TLP testing is like curve-tracing for ESD events

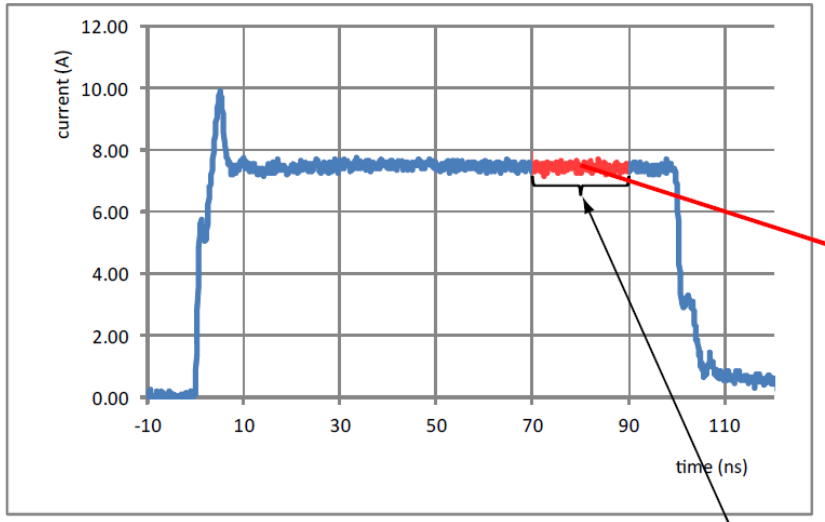


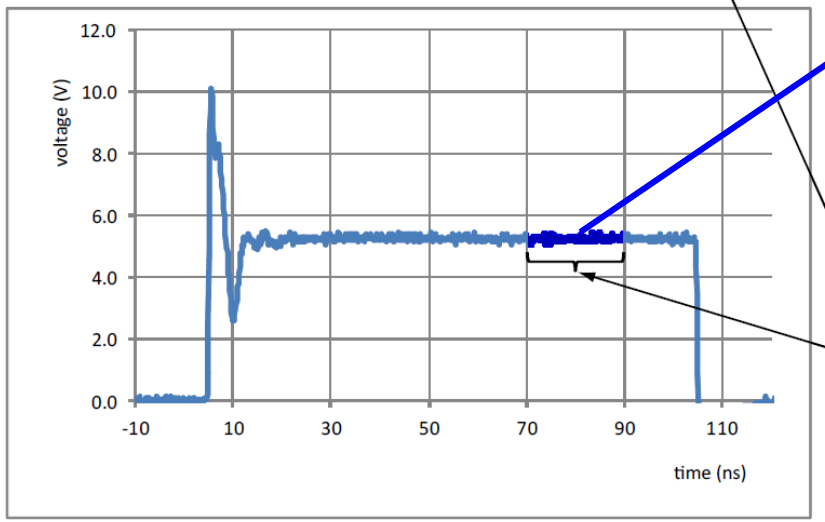
ESD performance can be judged exactly, based on TLP curve measurements

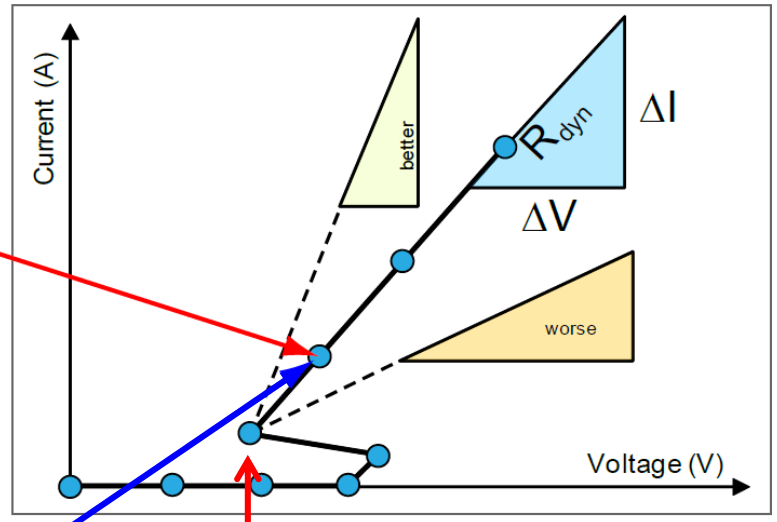
TLP measurement (2), how to derive a TLP curve

Transmission Line Pulse

- Typical pulse width 100ns
- VF-TLP (very fast) ~5ns





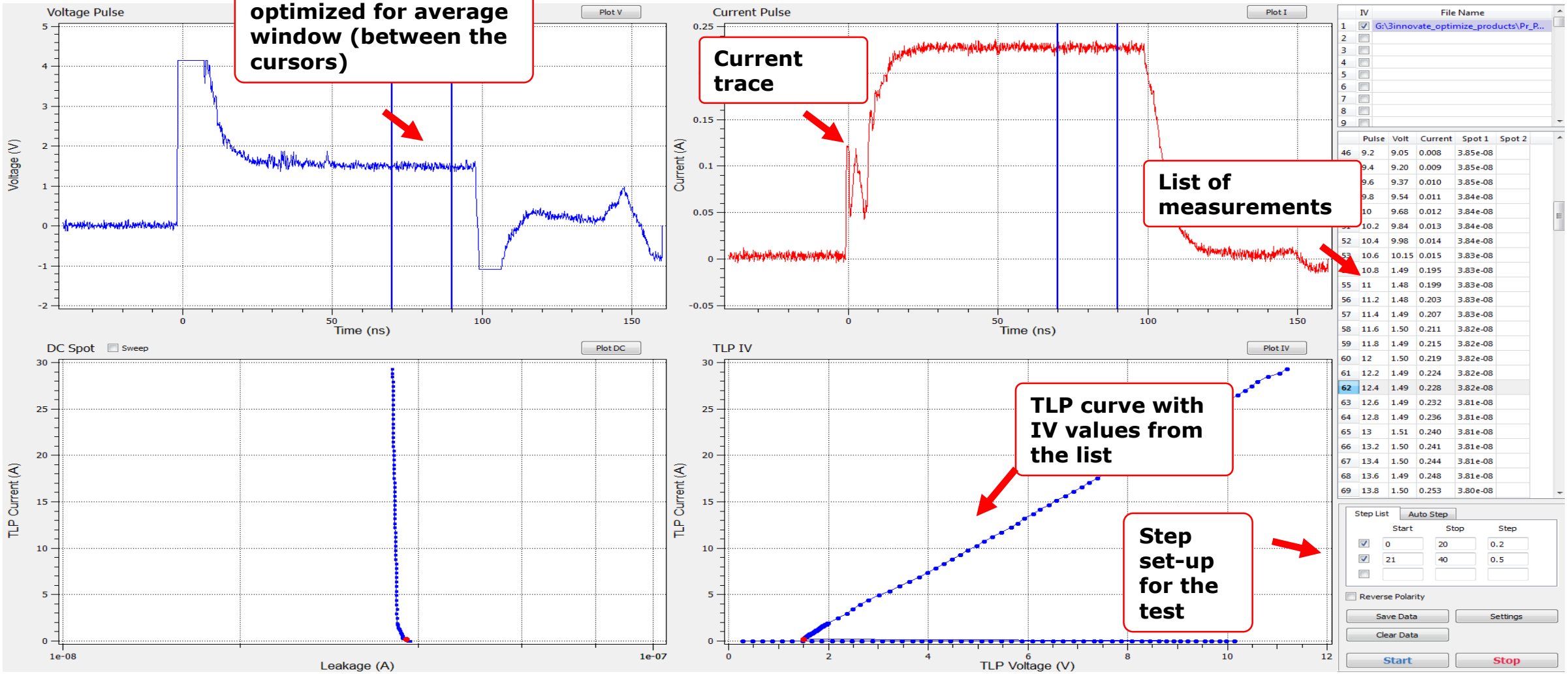


$V_{snap\text{-}back}$

The dynamic resistance R_{dyn} is derived from the steepness of the TLP graph: $\Delta V / \Delta I$

For each TLP measurement voltage and current samples are averaged over 20 ns and denoted as single point in the TLP graph.

TLP Test – measurement results



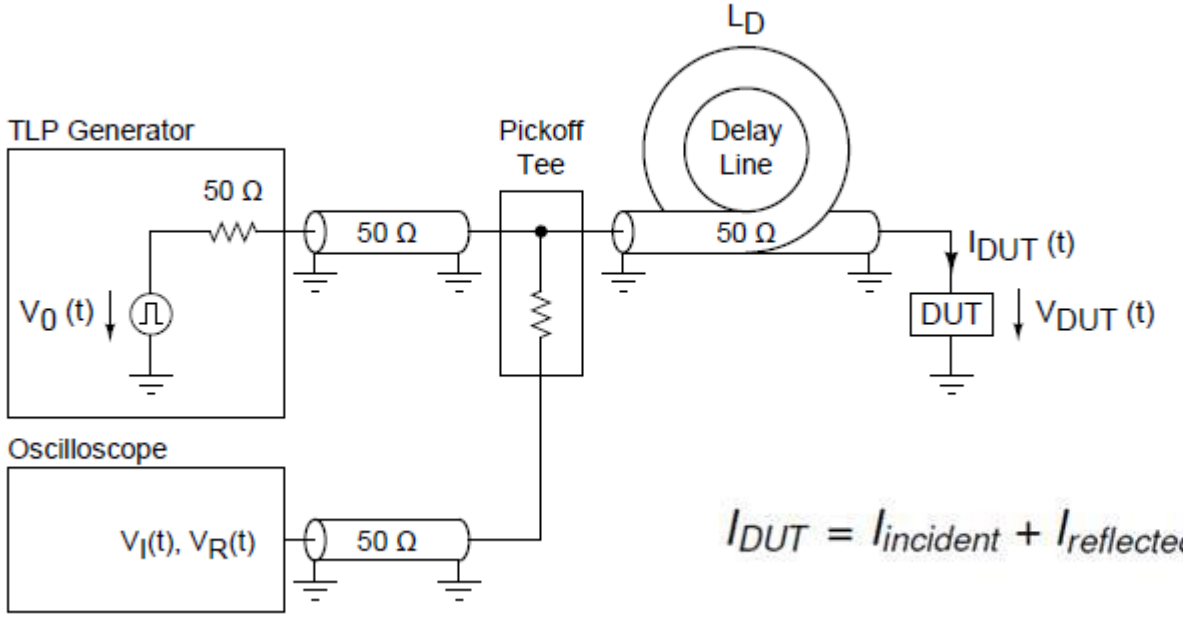
VF-TLP (Very Fast TLP) measurement

Using pulse widths < 10 ns, steep rise/fall times

Better characterization of the switch-on time of the protection diode

Incident and reflected signal are measured separately

(TDR principle, direct current probe is too slow to handle the short pulses)



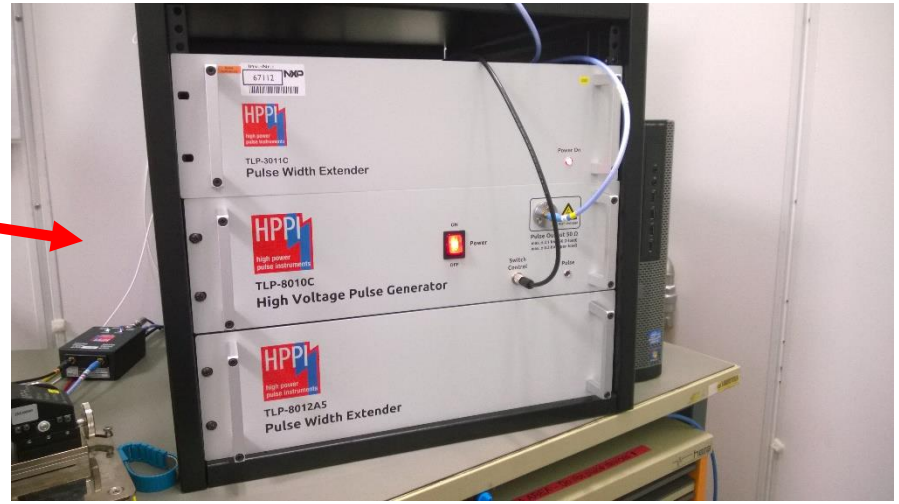
$$I_{DUT} = I_{incident} + I_{reflected} = \frac{V_{incident} - V_{reflected}}{50\,\Omega}$$

TLP Test – Set up for component testing

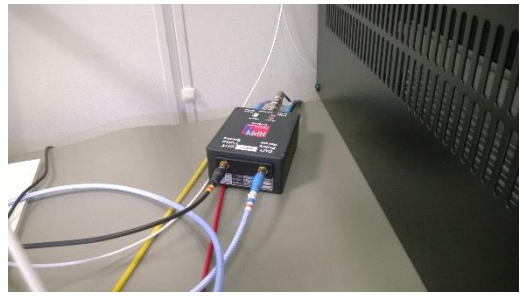
HPPI TLP generator

Generator

2 pulse width extender



Switch-box



Microscope for needle testing

With micro manipulators

Two needle pairs for powerless

sense

Needle probes

DUT is put backside down on an ceramic insulator tile. The 2 needle pairs are contacted directly (signal pad; ground pad)

TLP measurement (4), selection of a suitable protection

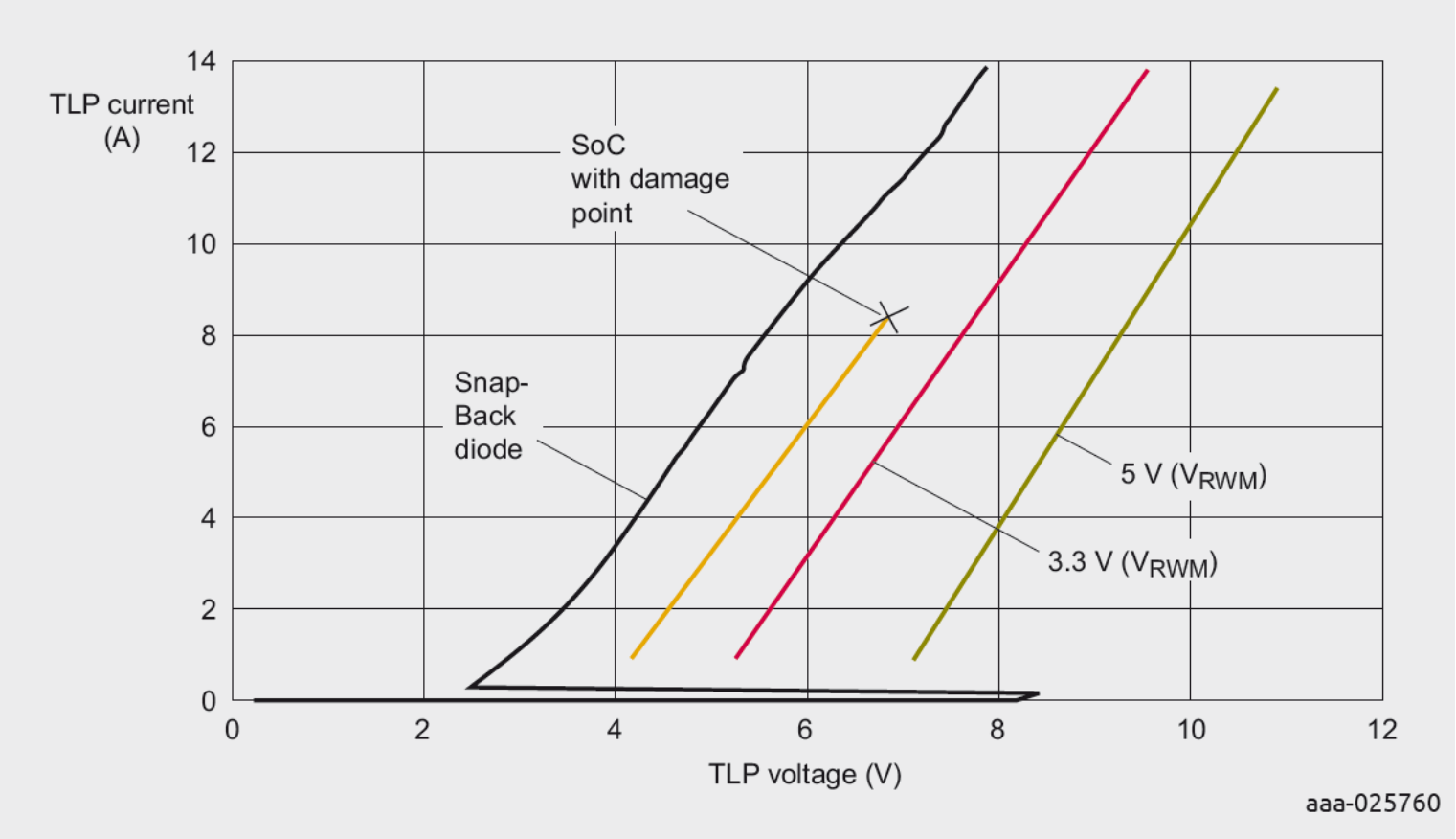


Figure 23 | TLP-Curves of avalanche type ESD diodes with VRWM5 V (green), Vrwm 3.3 V (red),

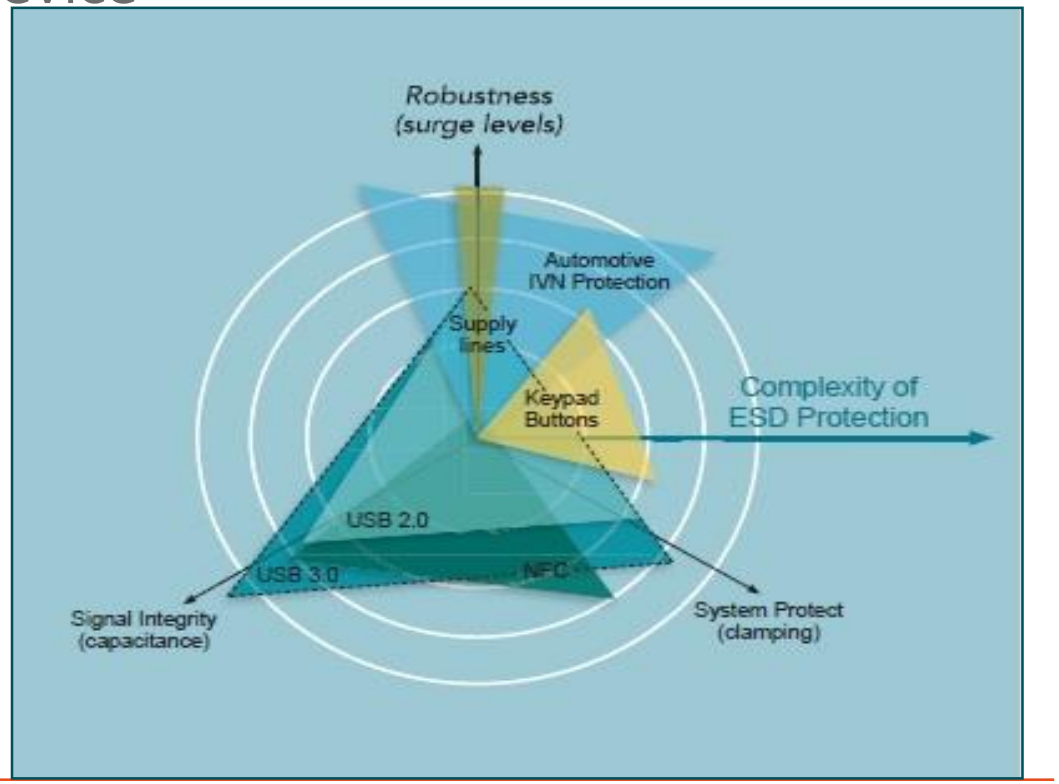
Ω

Selection criteria for ESD protection, Findings for super-speed interfaces

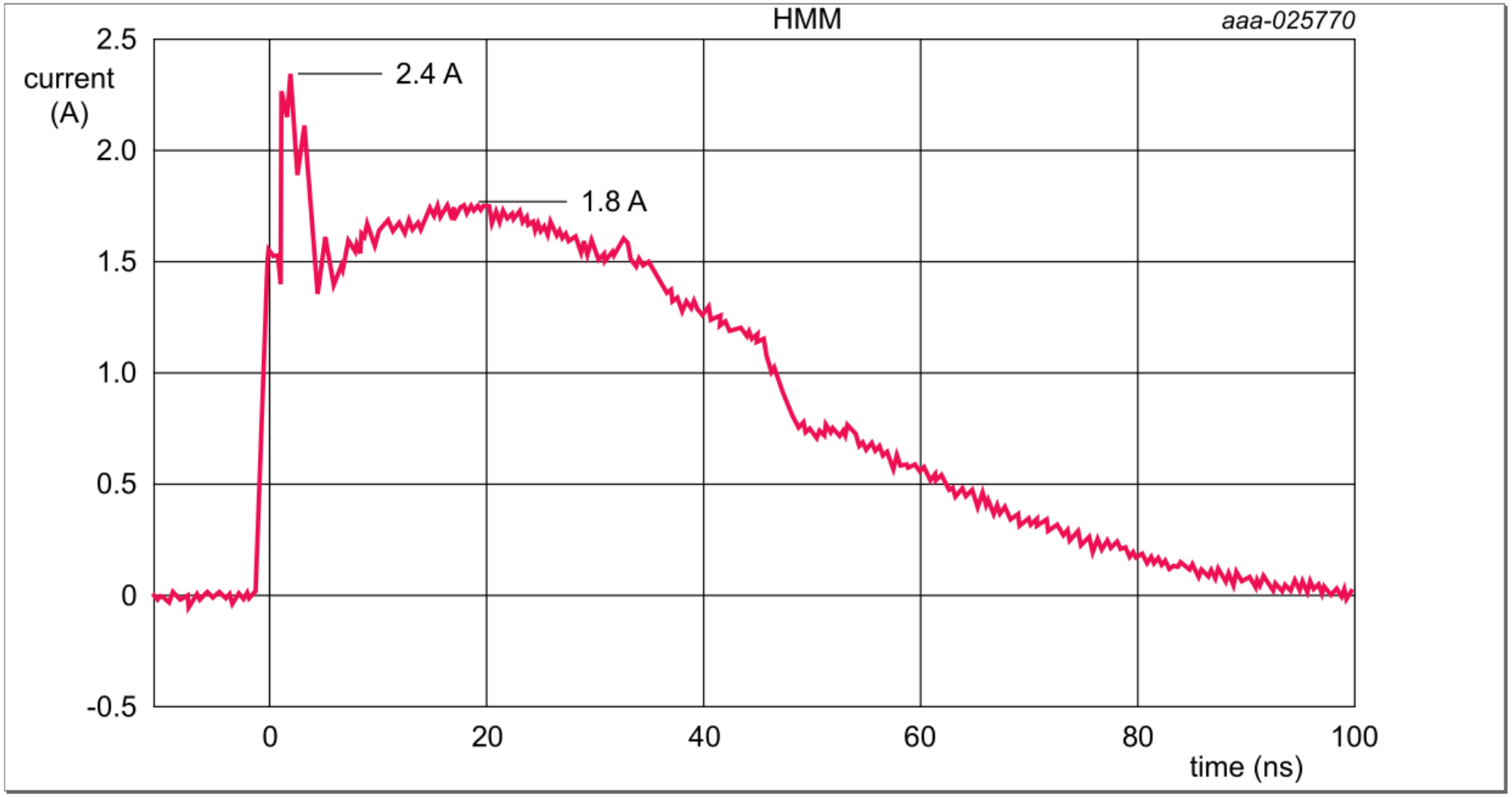
ESD – External ESD Protection

Selection Criteria for Protection Devices

- Number of signal lines
- Package (shape/size/footprint) of protection device
- Reverse stand-off voltage V_{RWM}
- ESD robustness level V_{ESD}
- Clamping voltage V_{clamp}
- Dynamic resistance R_{dyn}
- Topology: uni- / bi-directional, rail to rail, …
- Device capacitance C_{diode} and other parasitics

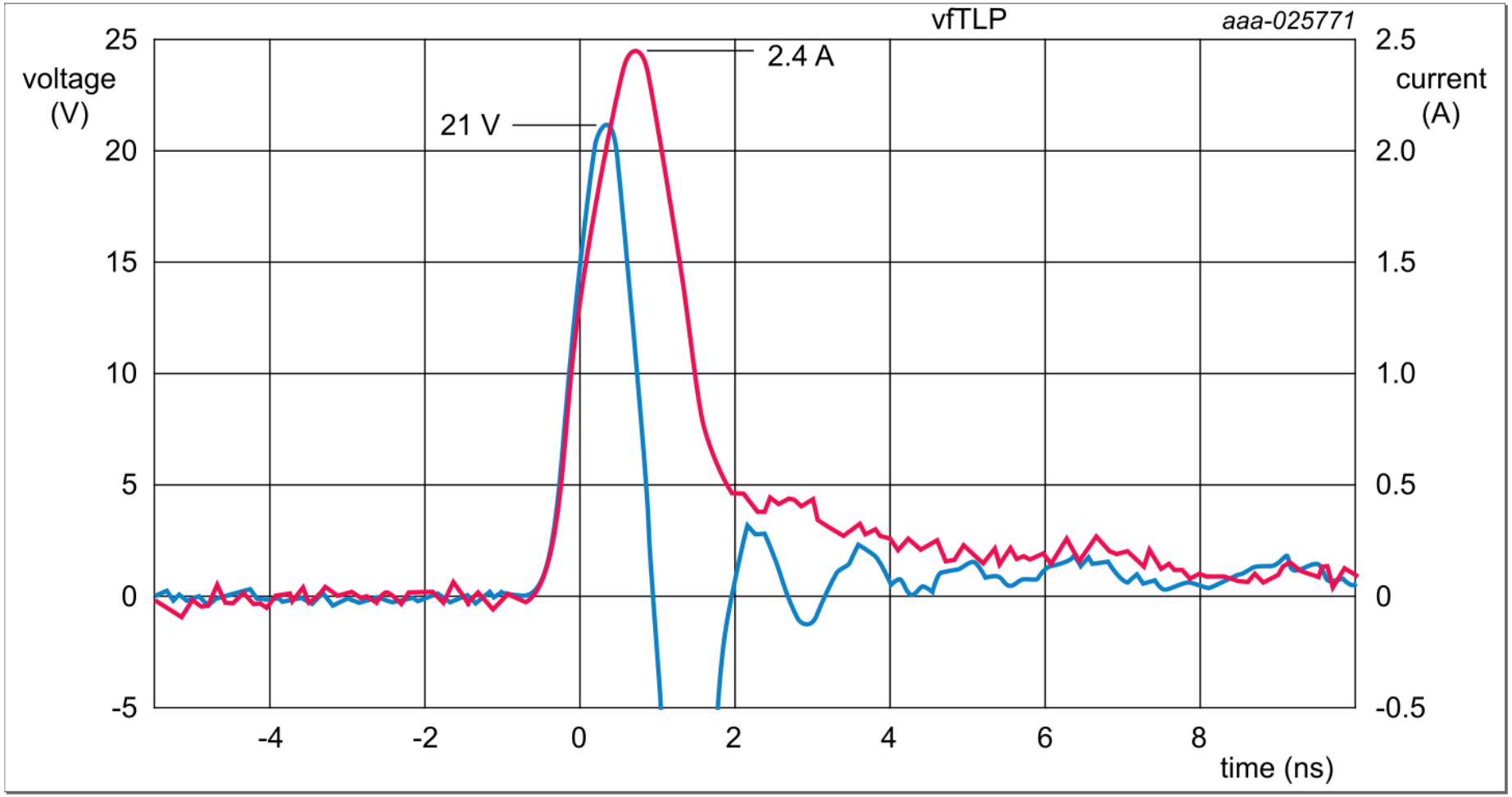


ESD test of an extremely sensitive USB interface with an HMM test



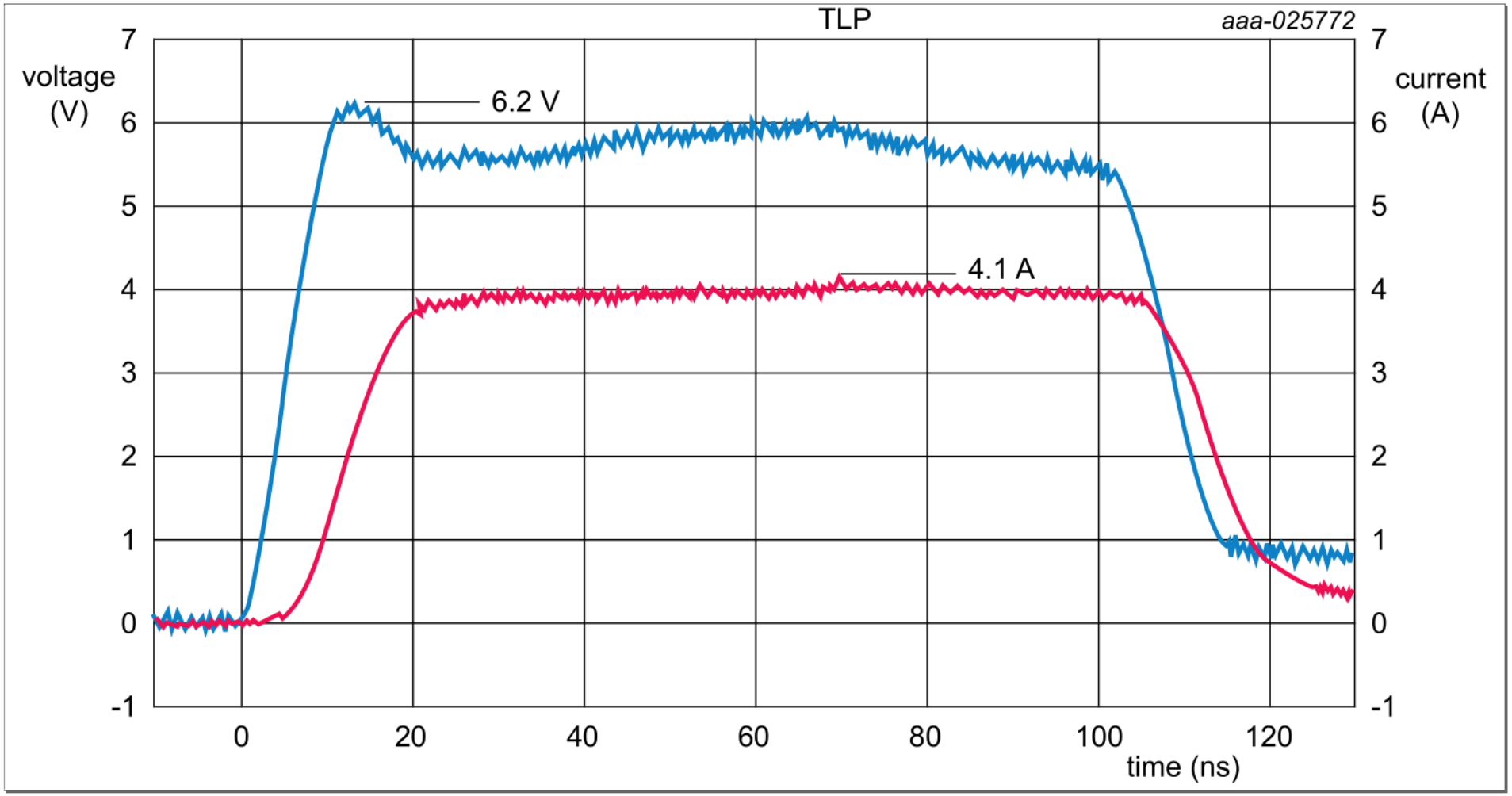
Pulse form at SoC Limit

vfTLP test for the extremely sensitive USB interface



test
at SoC
limit

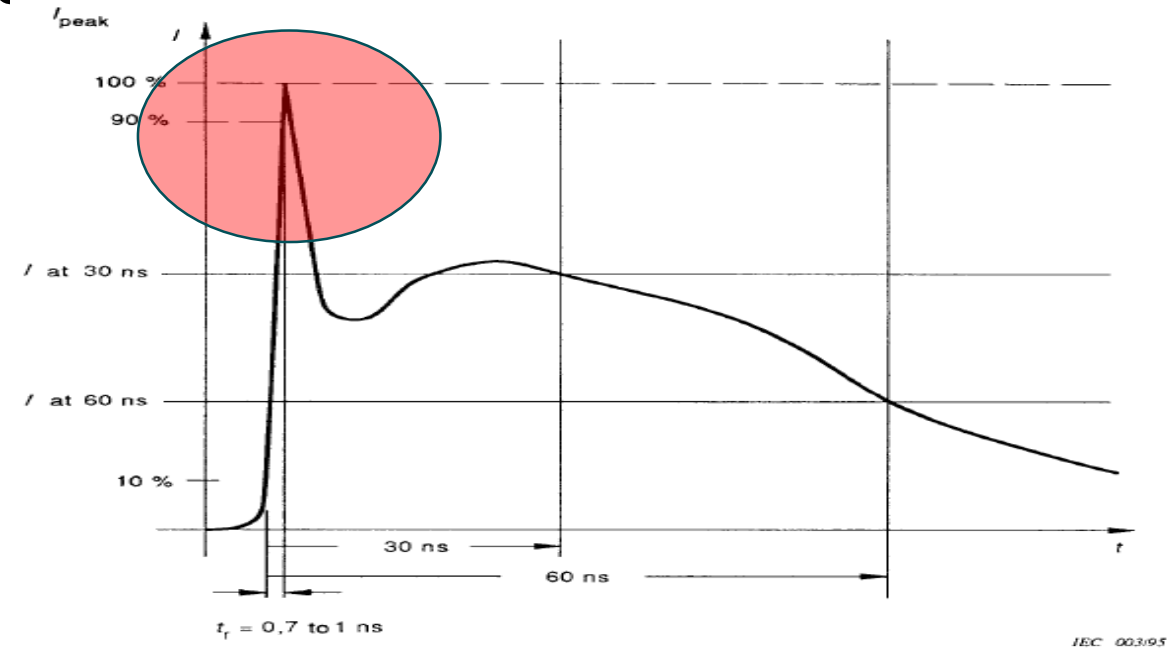
TLP test for the extremely sensitive USB interface



test
at SoC
limit

TLP test for the extremely sensitive USB interface

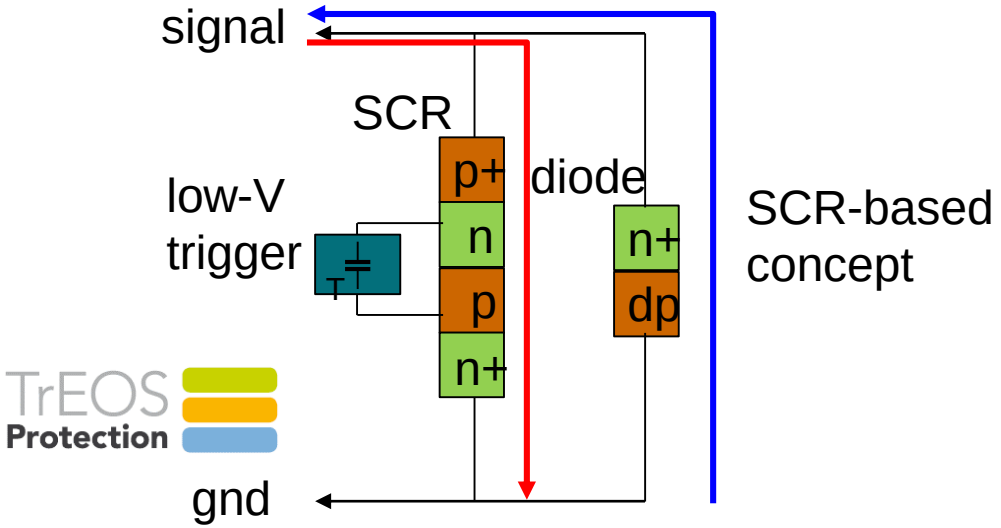
Finding: SoC is damaged from first overshoot of an ESD strike and not the second shoulder.
Conclusion: the damping of this first overshoot has become an importa for ESD protection products !

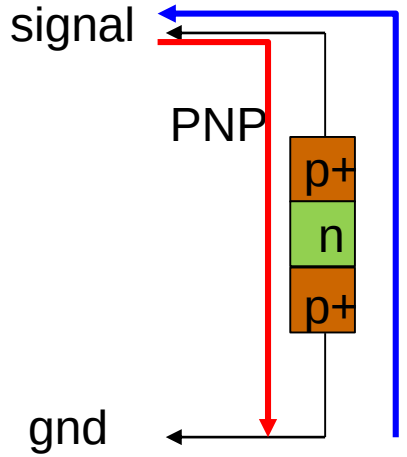


Topology of snap-back ESD protection devices

Snap-Back Technologies

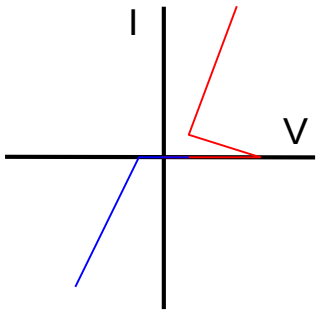
SCR versus Open-Base PNP Transistor





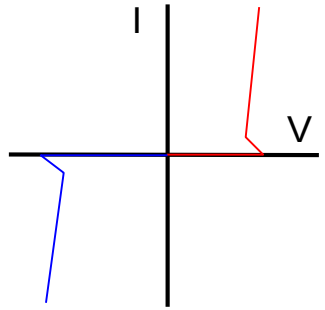
SCR-based

- reverse diode
- very low snapback
- high surge capability
- low Rdyn / C

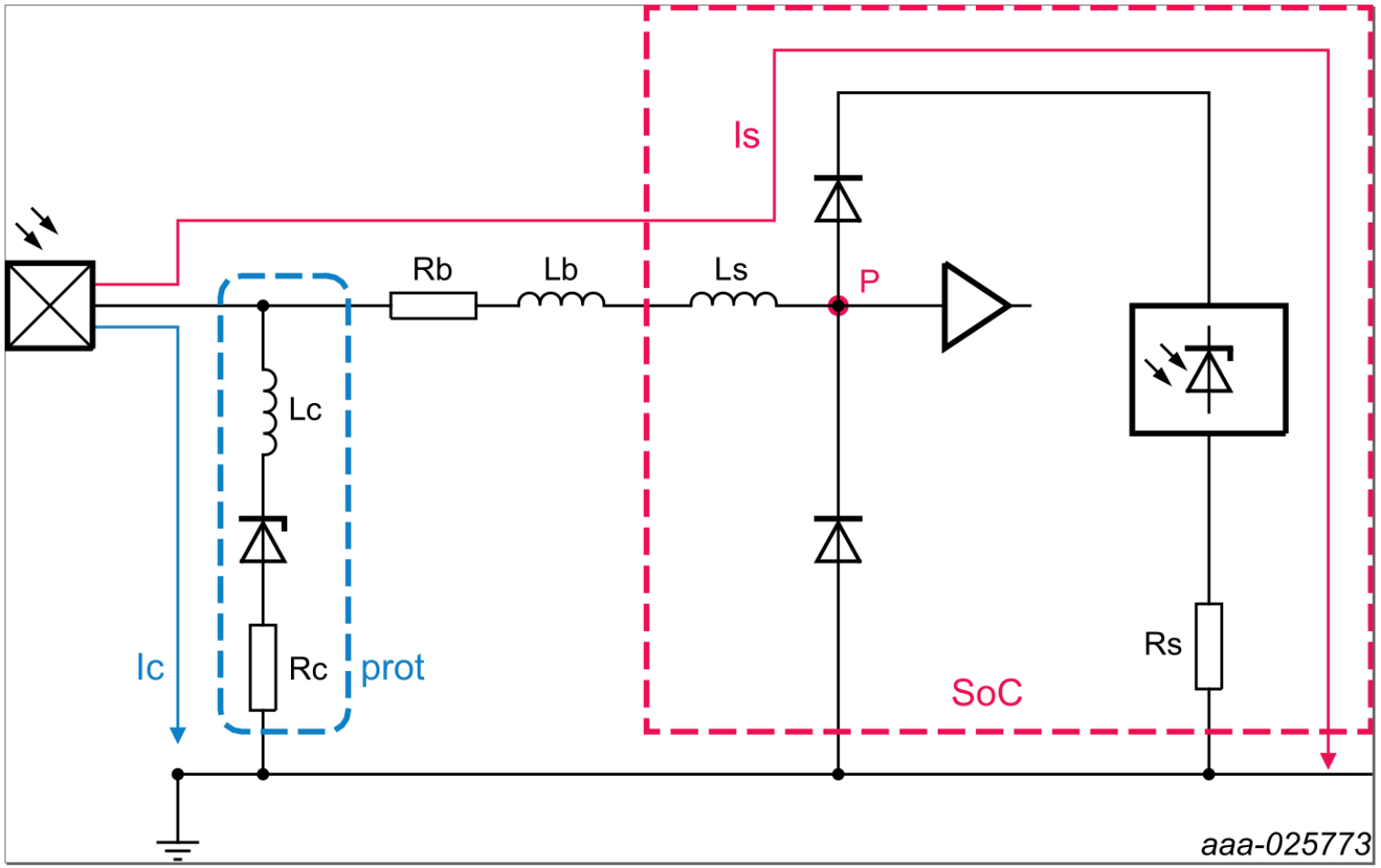


open-base PNP

- 'symmetric'
- small snapback
- latch-up robust
- low Rdyn / C



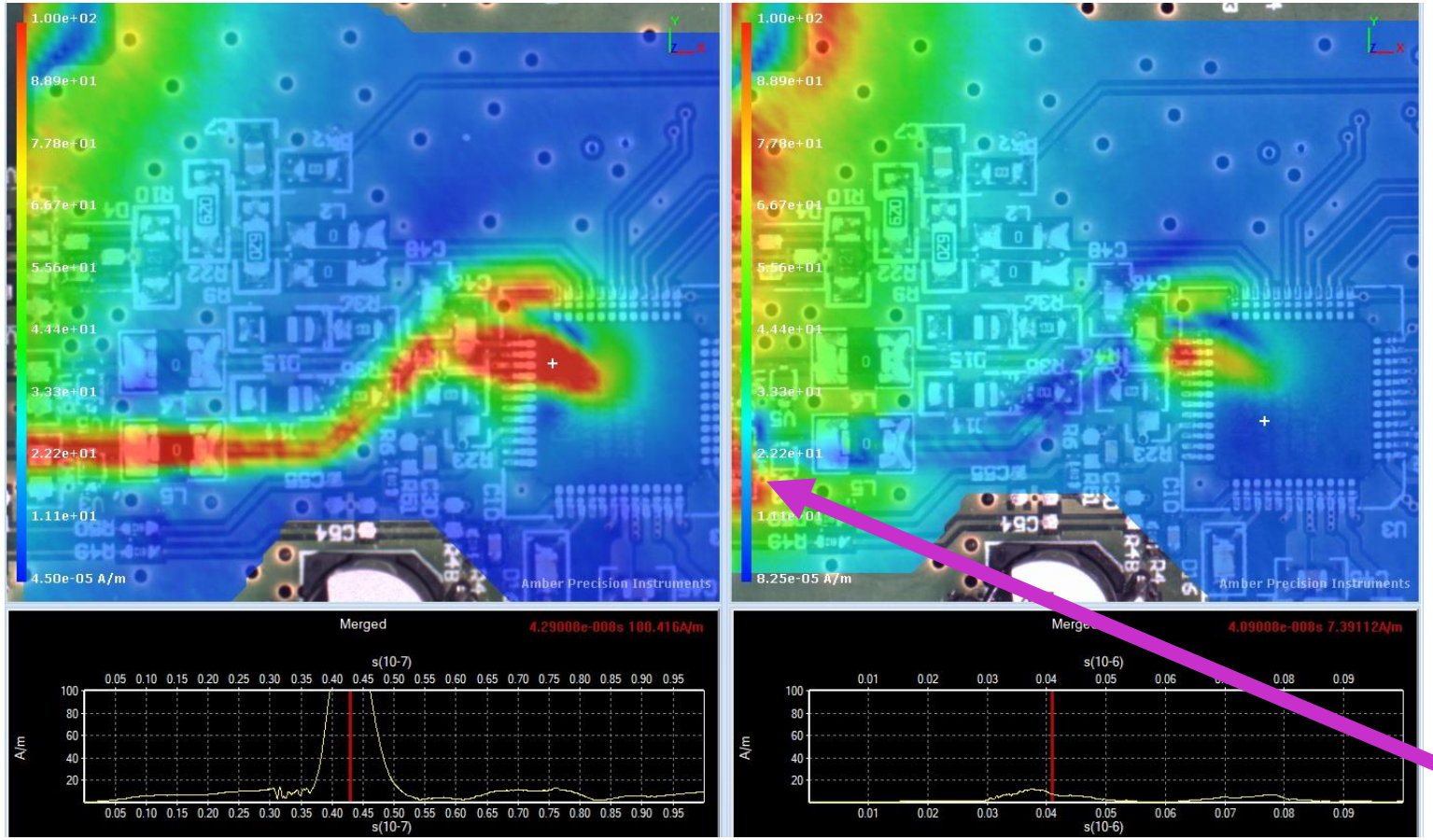
System Efficient ESD Design (SEED)



EMI - Scanner

Example CAN Transceiver Reference PCB

Without protection



With protection

PESD2IVN24-T

New ESD protection products (TrEOS 2)

Type	Capacitance (typical, pF @ 0V)	ESD ruggedness (kV)	Polarity	Package	Remark
PES2V0Y1BSF	0.69	20	Bidirectional	DSN0603 / SOD962	Single line, ESD protection
PES2V5Y1BSF	0.25	16	Bidirectional	DSN0603 / SOD962	Single line, ESD protection
PES3V3Y1BSF	0.26	16	Bidirectional	DSN0603 / SOD962	Single line, ESD protection
PES4V0Y1BSF	0.26	16	Bidirectional	DSN0603 / SOD962	Single line, ESD protection
				SOT1176	

Advantages of TREOS2 products:

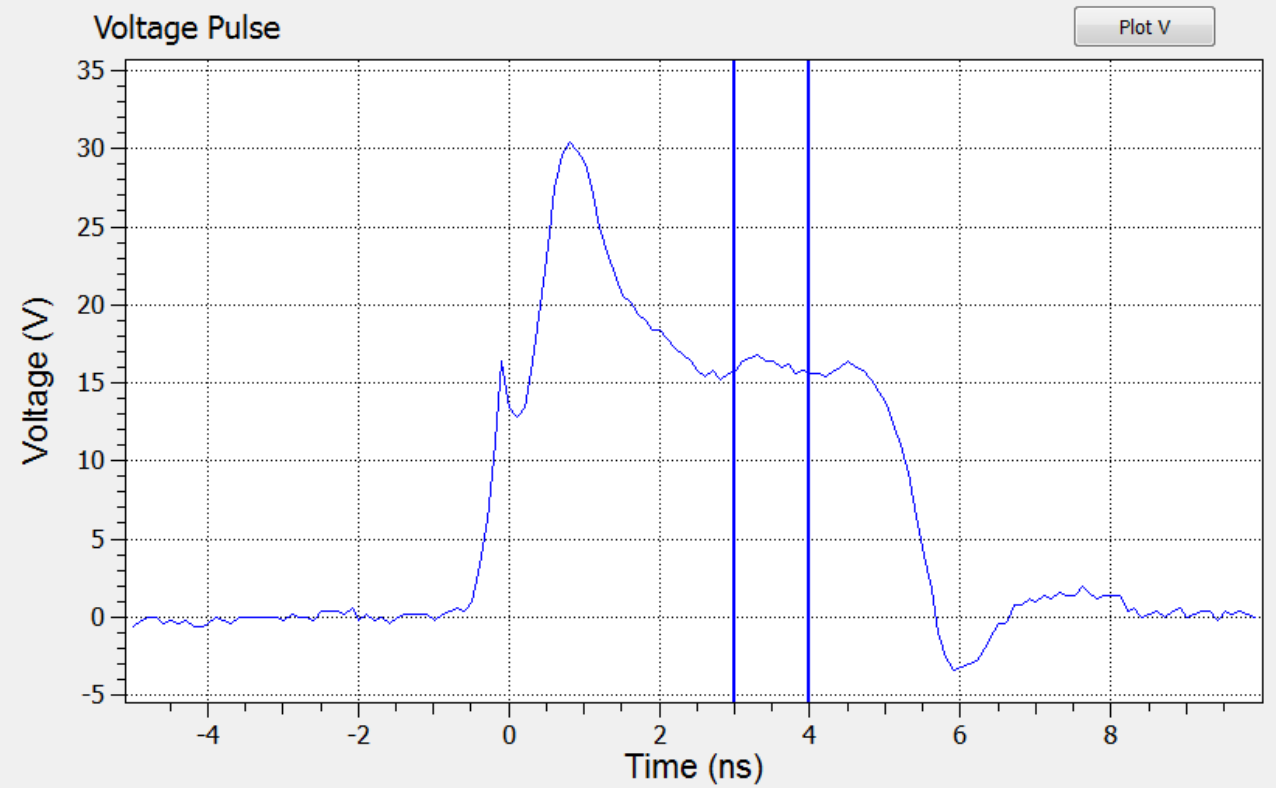
- **Ultra fast turn-on**
- **Good damping of first overshoots**
- **Deep snapback -> ultra low Vclamp**
- **Low Rdyn**
- **Higher ESD robustness level**

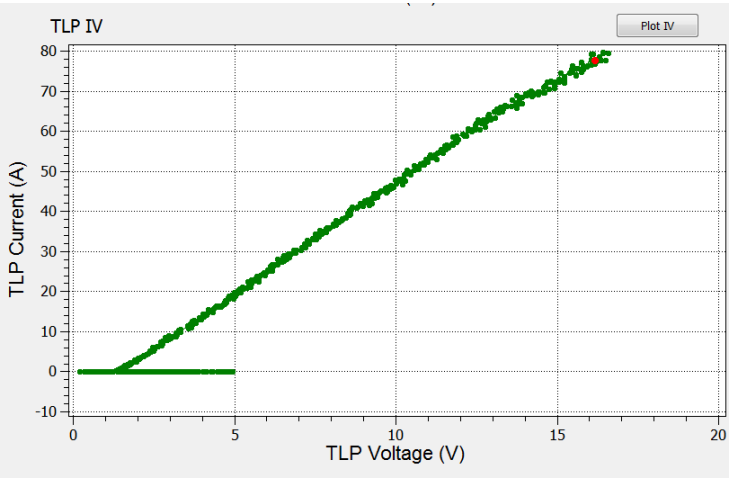
New ESD protection products (TrEOS 2)

TrEOS Protection

TrEOS 2 example PESD2V0Y1BSF, VF-TLP 4 kV pulse

Clamping curve





VF-TLP Curve, Td = 5ns, tr = 600 ps

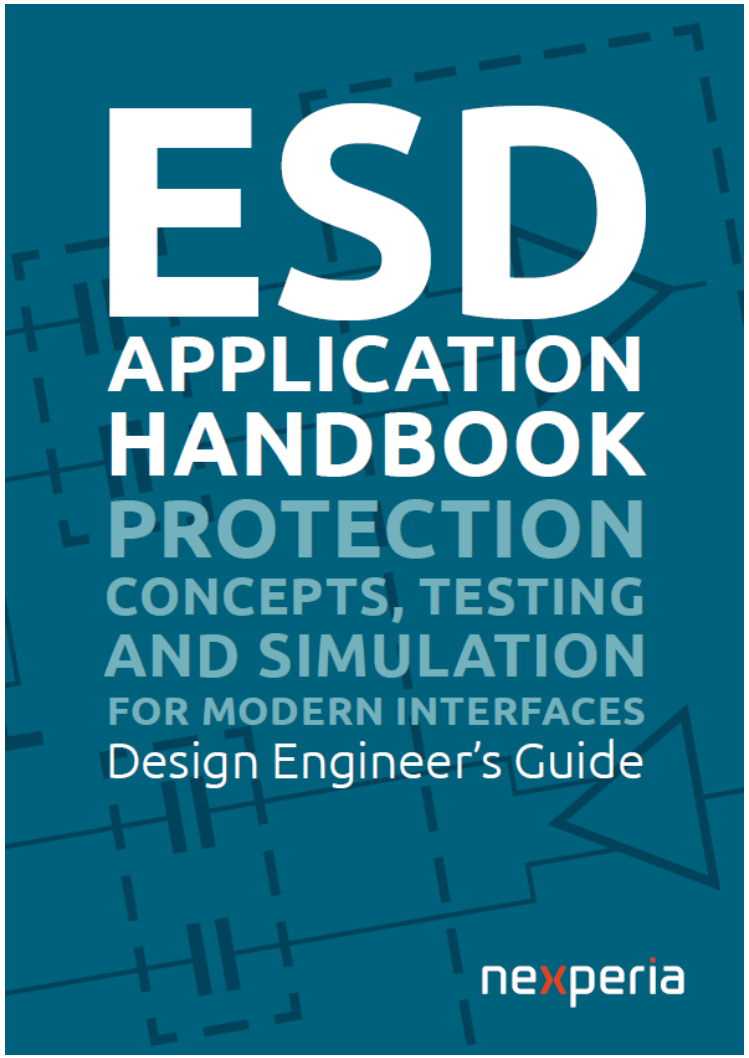
	Pulse	Volt	Current
621	3970	16.05	76.562
622	3980	16.11	79.335
623	3990	16.04	77.653
624	4000	16.15	77.798
625	4010	16.20	77.555
626	4020	16.16	76.889

4kV clamped down to 16.15 V and 30V peak, Ipp ~ 78 A

ESD application handbook

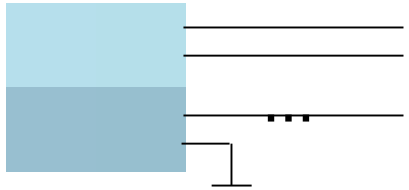
Design Engineer's Guide

- Release of final PDF August 31st
- Available on Nexperia Website:
- https://efficiencywins.nexperia.com/efficient-products/esd-design-engineers-guide.html
- Print out version available beginning of October



Common mode filters with integrated ESD protection

Common Mode Chokes (1)

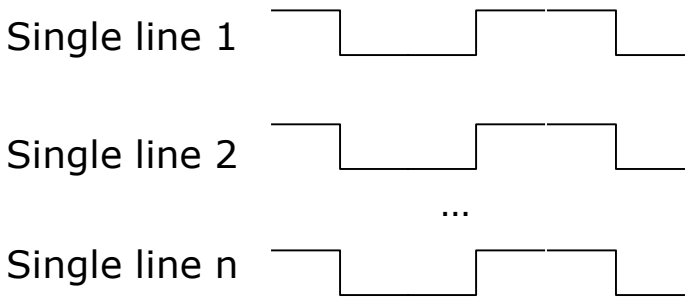


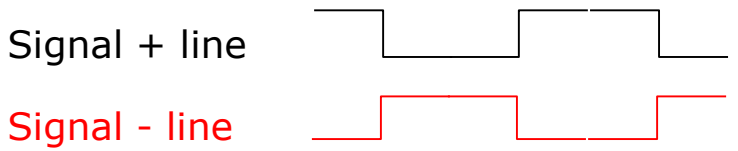
Single-ended Interface

- Data signal defined via voltage vs ground
- EMI added to the signal line
- Filter concepts are RC and LC low-pass filters

Differential Interface

- Data signal defined via differential voltage
  on a line pair (differential receivers)
- EMI is added to both of the differential signal parts
- Filter concept of the choice are Common Mode filters

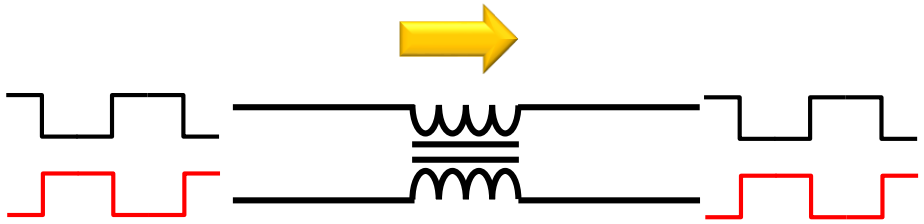




Modern high-speed and low-voltage interfaces work in differential mode

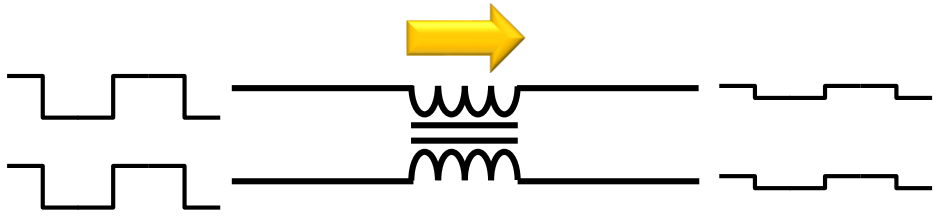
Common Mode Chokes (2)

Differential signal



Common mode choke

Common Mode signal



Common mode choke

Common Mode Chokes

- Common Mode Chokes let:

  differential signals pass, but

  suppress common-mode noise

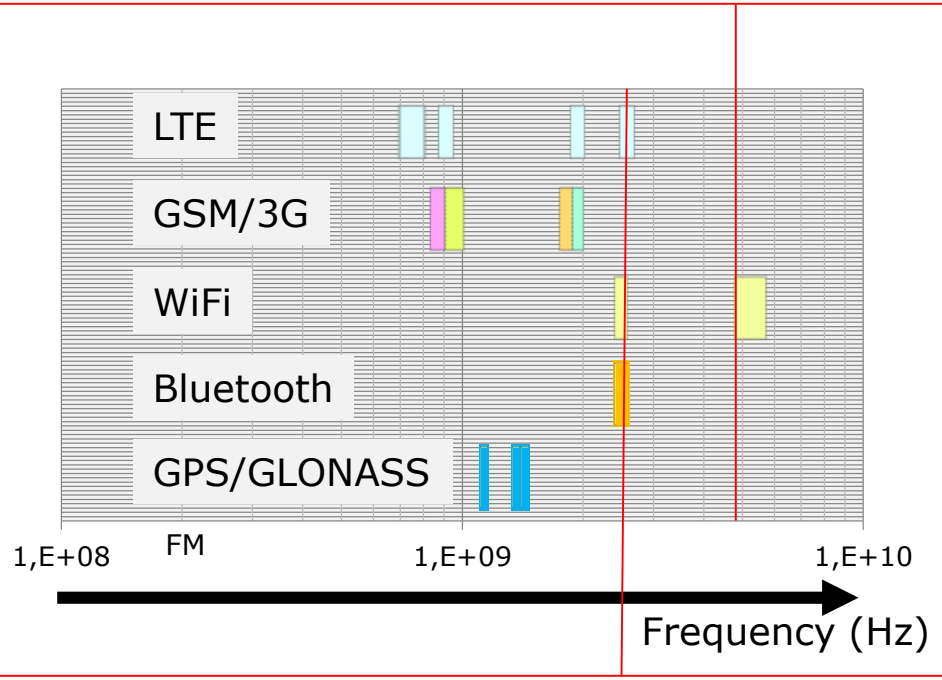
High-speed Interfaces

- Serial data increase data rates
- Reduced line count (less complex connectors, cables and PCB layout)
- Low level differential signals (less radiation and EMC, reliable data transmission)

Common Mode chokes suppress common noise in differential signals

Critical frequencies in combination with USB3.1

USB3.1 @10 Gbit/s fundamental (5 GHz)



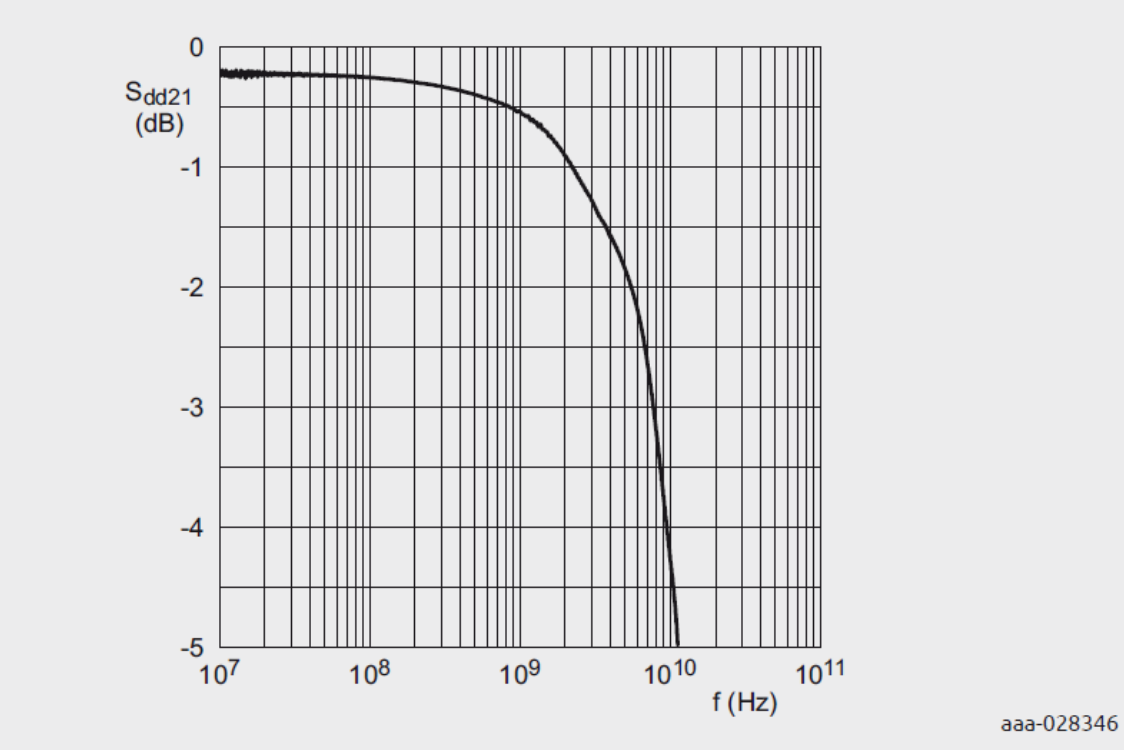
USB3.1 @5 Gbit/s fundamental (2.5 GHz)

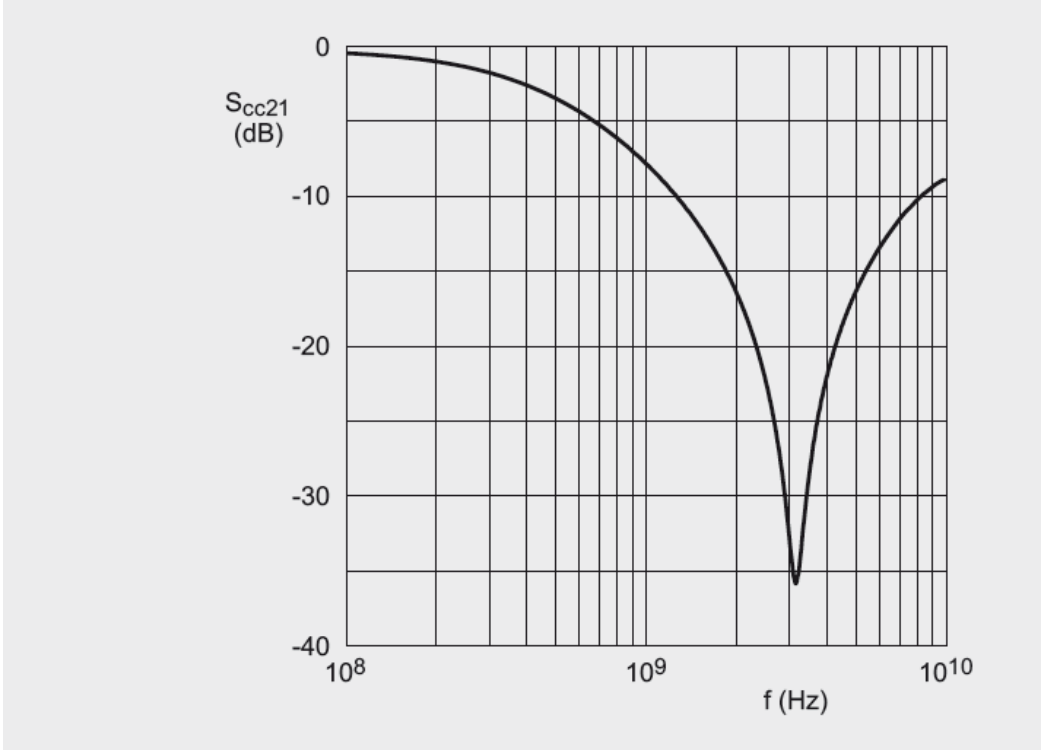
For wireless connectivity, portable devices have wireless transmitters, which operate in the same frequency bands as fast data lines, such as USB3.1

- GSM 850 – up 824-849 MHz
- GSM 850 – dwn 869-894 MHz
- GSM 900 – up 890-915 MHz
- GSM 900 – dwn 935-960 MHz
- GSM 1800 – up 1710-1785 MHz
- GSM 1800 – dwn 1805-1880 MHz
- GSM 1900 – up 1850-1910 MHz
- GSM 1900 – dwn 1930-1990 MHz
- WIFI 2.4 – 2.5 GHz
- WIFI 4.9 – 5.8 GHz
- Bluetooth, 2.4-2.5 GHz
- GPS 1.2, 1.5 GHz, GLONASS 1.6 GHz
- LTE 700/800 MHz, 1700/1900 MHz
- LTE 900 MHz, 1.8, 1.9, 2.5, 2.6 GHZ

USB Type-C

- PCMFxUSB3B , differential passband and common mode rejection



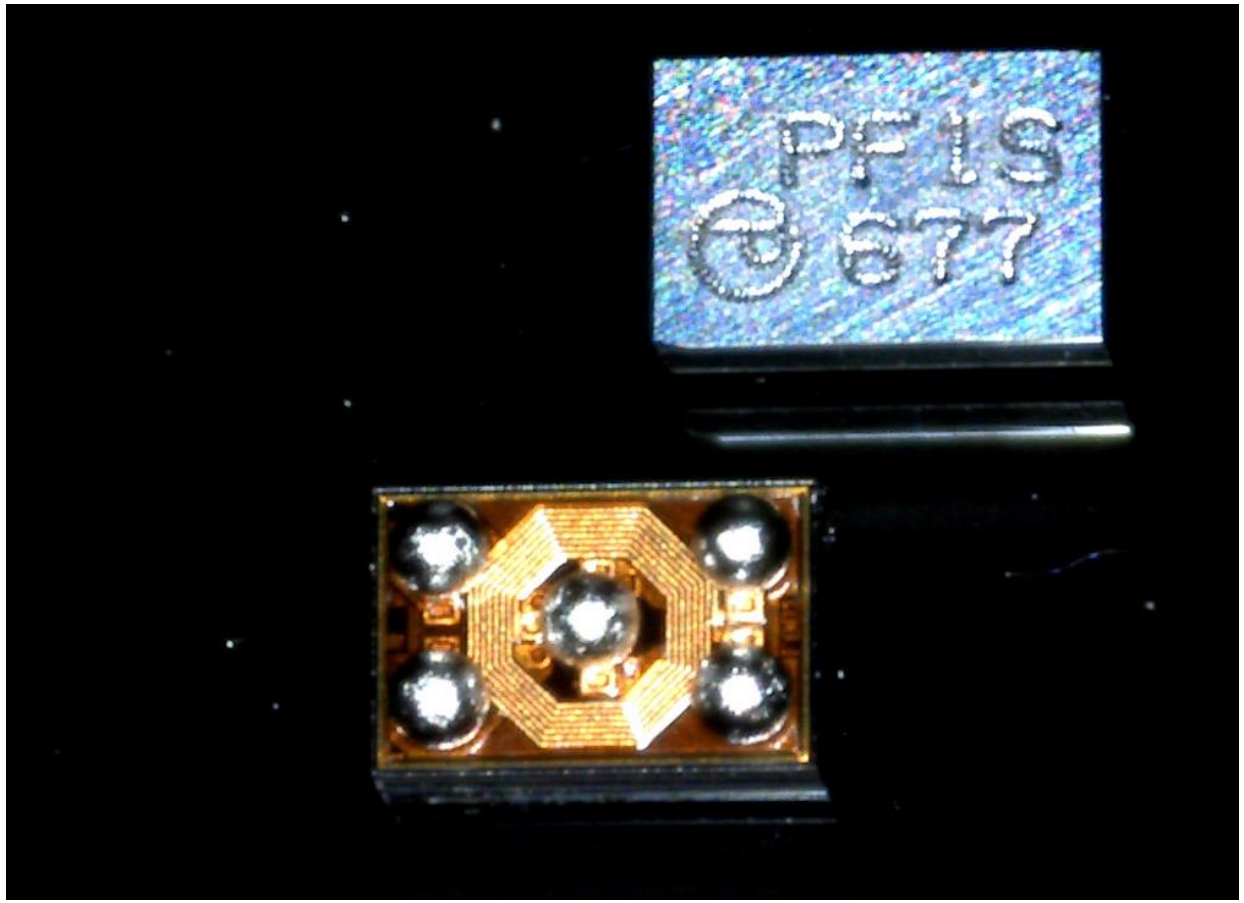


USB Type-C

PCMF1USB3B , microscope pictures

WLCSP Packages
5,10 or 15 balls

For 1, 2 or 3 lanes



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