Nexperia

Aktuelle Trends in Signalschutz und -filterung digitaler Datenübertragung
Agenda

• General aspects for ESD
• Testing methods - IEC61000, TLP, VF-TLP...
• ESD protection selection criteria for ESD protection, latest findings for super speed interfaces
• Topology of snap-back ESD protection devices
• Common Mode Filters with ESD protection
ESD – Electro Static Discharge

Material / environmental influences affect charge separation

Typical values for the electrostatic voltage to which a person can be charged when in contact with said materials.

- **Synthetic fibres**
- **wool**
- **Antistatic fibres**

Graph showing the relationship between relative humidity and electrostatic voltage (U in kV) for different materials. The graph indicates that low relative humidity (e.g. offices without humidity control in the winter) results in higher electrostatic voltages.
ESD – Defects caused by ESD

Destruction mechanism

High voltage

High energy

\[ \frac{1}{I_{\text{peak}}} \text{ in } \% \]

\[ I \text{ in } \text{A} \]

\[ \text{time in ns} \]

\[ T_{\text{rise}} \approx 1 \text{ ns} \]
ESD Damage – IC technology trend

- **Trend**: Chip size decreases to a minimum
  - Gate thickness and chip size (channel length) decreases
  - Maximum gate voltage decreases (e.g. for CMOS090 <1.5V static)
  - New Processes are optimized for area and performance, NOT for ESD performance!

- **Impact**: Modern ICs designs are very sensitive to ESD strikes
  - ICs failure due to gate oxide punch through from high voltages
  - ICs failure from Joule heating due to high residual currents
  - Additional board level ESD protection for external interfaces becomes a must!
## Super speed interfaces

### Data Speed Increase

<table>
<thead>
<tr>
<th>Table 7: Overview of data rates for USB interfaces</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>USB Type</strong></td>
</tr>
<tr>
<td>------------</td>
</tr>
<tr>
<td>USB 1.0</td>
</tr>
<tr>
<td>USB 1.0</td>
</tr>
<tr>
<td>USB 2.0</td>
</tr>
<tr>
<td>USB 3.0</td>
</tr>
<tr>
<td>USB 3.1</td>
</tr>
<tr>
<td>USB 3.2</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Table 22: List of HDMI key parameters f</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>HDMI version</strong></td>
</tr>
<tr>
<td>Maximum pixel clock rate (MHz)</td>
</tr>
<tr>
<td>Maximum TMDS bit rate per lane including 8b/10b coding overhead (Gbit/s)</td>
</tr>
<tr>
<td>Maximum total TMDS throughput including 8B/10b coding overhead (Gbit/s)</td>
</tr>
<tr>
<td>Maximum audio throughput bit rate (Mbit/s)</td>
</tr>
<tr>
<td>Maximum video resolution over 24 bit/pixel single link</td>
</tr>
<tr>
<td>Maximum color depth (bit/pixel)</td>
</tr>
</tbody>
</table>
Testing methods
ESD – Device Level Testing: HBM

Human Body Model

- HBM was developed to simulate the discharge of a human body to a grounded device (IC).
- To replicate an RC network is used:
  - $R_{\text{discharge}} = 1500$ ohms
  - $C = 100$ pF
- ANSI / ESDA / JEDEC JS-001-2012 for Semiconductor Components
- Different from standard EN 61000-4-2 for devices (system level test)
ESD – Device Level Testing: CDM
Charged Device Model

• CDM emulates the process of charging / discharging that can occur in production environments.

• For example, ICs that are poured from plastic tubes and hit a metallic surface.

• It is conceivable that charges have accumulated on the metal pins of an IC or on the package, ultimately discharging through a single grounded pin.

• The discharge current is limited only by parasitic impedances and capacitance.
ESD – System Level Testing: IEC 61000-4-2

Typical waveform of ESD current

- **Rise time**
  - 0.7 – 1 ns (von 10% auf 90%)

- **Peak current**
  - +/- 10% tolerance

- **Current after 30 ns**
  - +/- 30% tolerance

- **Current after 60 ns**
  - +/- 30% tolerance

<table>
<thead>
<tr>
<th>Applied Voltage in kV</th>
<th>Peak Current Human Body Model in A</th>
<th>Peak Current IEC 61000-4-2 in A</th>
<th>Current at 30 ns</th>
<th>Current at 60 ns</th>
</tr>
</thead>
<tbody>
<tr>
<td>2</td>
<td>1.33</td>
<td>7.5</td>
<td>4</td>
<td>2</td>
</tr>
<tr>
<td>4</td>
<td>2.66</td>
<td>15.0</td>
<td>8</td>
<td>4</td>
</tr>
<tr>
<td>6</td>
<td>4.00</td>
<td>22.5</td>
<td>12</td>
<td>6</td>
</tr>
<tr>
<td>8</td>
<td>5.33</td>
<td>30.0</td>
<td>16</td>
<td>8</td>
</tr>
<tr>
<td>10</td>
<td>6.66</td>
<td>37.5</td>
<td>20</td>
<td>10</td>
</tr>
</tbody>
</table>
ESD – System Level Testing: IEC 61000-4-2

Simplified equivalent circuit diagram of ESD test generator

- **R\text{charge}** (Mega Ohms)
- **R\text{discharge}** (330 Ohms)
- **C\text{charge}** (150 pF)

DC High Voltage supply

DUT (device under Test)

Discharge Tip

Ground return
ESD pulse waveform variation (1)

NoiseKen gun monitored with F-65 current probe
ESD pulse waveform variation (2)

NoiseKen gun monitored with F-65 current probe, shots on 2 Ohm Pellegrini target

Waveforms compliant To IEC61000-4-2,
Good reproducibility

Figure 2 Repeated NoiseKen 1 kV current waveforms into a Pellegrini target.
ESD pulse waveform variation (3)

NoiseKen gun monitored with F-65 current probe, shots at PC system target

Reference is IEC 61000-4-2
1st peak 3.75 A ± 15 %
2nd peak 2A ± 30 %

2nd peak stable and in spec
1st peak -35 % to +25 % variation out of specification

aaa-025744
ESD stray pulses

Nexperia recommends to short the gun to GND before contacting the target, then remove the ground connection and start to shoot.

![Graph showing ESD stray pulses](image)

- **target = 3.75 A**
- **time (ns)**
- **Pellegrini**
- **Stray pulse**

![Diagram of ESD circuit](image)

- 50 MΩ
- 330 Ω
- 150 pF
- 40 pF
- Ltip
- Ct
- Lg
- Cg
- HV
- Rd
- DUT

aaa-025746
ESD performance can be judged exactly, based on TLP curve measurements

**Principle of TLP Measurement**

- Device under Test (DUT) is subjected to rectangular current pulses
- Duration of these pulses is between 5ns – 100 ns.
- The current is increased step by step, until the system starts to show a failure
- Connecting the results to an $I_{DUT}$ versus $V_{DUT}$ curve describes the response of a system for ESD surge events
- TLP testing is like curve-tracing for ESD events
TLP measurement (2), how to derive a TLP curve

Transmission Line Pulse

- Typical pulse width 100ns
- VF-TLP (very fast) ~5ns

The dynamic resistance $R_{\text{dyn}}$ is derived from the steepness of the TLP graph: $\Delta V / \Delta I$

For each TLP measurement voltage and current samples are averaged over 20 ns and denoted as single point in the TLP graph.
TLP Test – measurement results

Voltage trace, scope optimized for average window (between the cursors)

Current trace

List of measurements

TLP curve with IV values from the list

Step set-up for the test
VF-TLP (Very Fast TLP) measurement

Using pulse widths < 10 ns, steep rise/fall times
Better characterization of the switch-on time of the protection diode
Incident and reflected signal are measured separately
(TDR principle, direct current probe is too slow to handle the short pulses)

\[ I_{DUT} = I_{\text{incident}} + I_{\text{reflected}} = \frac{V_{\text{incident}} - V_{\text{reflected}}}{50 \, \Omega} \]
TLP Test – Set up for component testing

HPPI TLP generator
Generator
2 pulse width extender

Microscope for needle testing
With micro manipulators
Two needle pairs for powerless sense

Switch-box

Needle probes
DUT is put backside down on an ceramic insulator tile. The 2 needle pairs are contacted directly (signal pad; ground pad)
TLP measurement (4), selection of a suitable protection

Figure 23 | TLP-Curves of avalanche type ESD diodes with VRWM5 V (green), Vrwm 3.3 V (red),
Selection criteria for ESD protection, Findings for super-speed interfaces
ESD – External ESD Protection

Selection Criteria for Protection Devices

- Number of signal lines
- Package (shape/size/footprint) of protection device
- Reverse stand-off voltage $V_{RWM}$
- ESD robustness level $V_{ESD}$
- Clamping voltage $V_{\text{clamp}}$
- Dynamic resistance $R_{\text{dyn}}$
- Topology: uni- / bi-directional, rail to rail, ...
- Device capacitance $C_{\text{diode}}$ and other parasitics
ESD test of an extremely sensitive USB interface with an HMM test

Pulse form at SoC Limit
vfTLP test for the extremely sensitive USB interface

test at SoC limit
TLP test for the extremely sensitive USB interface

test
at SoC
limit
TLP test for the extremely sensitive USB interface

Finding: SoC is damaged from first overshoot of an ESD strike and not the second shoulder.
Conclusion: the damping of this first overshoot has become an important target for ESD protection products!
Topology of snap-back ESD protection devices
Snap-Back Technologies

SCR versus Open-Base PNP Transistor

**SCR-based**
- reverse diode
- very low snapback
- high surge capability
- low $R_{dyn}/C$

**open-base PNP**
- 'symmetric'
- small snapback
- latch-up robust
- low $R_{dyn}/C$
System Efficient ESD Design (SEED)
**EMI - Scanner**

Example CAN Transceiver Reference PCB

Without protection

With protection

PESD2IVN24-T
### Advantages of TREOS2 products:
- Ultra fast turn-on
- Good damping of first overshoots
- Deep snapback -> ultra low Vclamp
- Low Rdyn
- Higher ESD robustness level

### New ESD protection products (TrEOS 2)

<table>
<thead>
<tr>
<th>Type</th>
<th>Capacitance (typical, pF @ 0V)</th>
<th>ESD ruggedness (kV)</th>
<th>Polarity</th>
<th>Package</th>
<th>Remark</th>
</tr>
</thead>
<tbody>
<tr>
<td>PES2V0Y1BSF</td>
<td>0.69</td>
<td>20</td>
<td>Bidirectional</td>
<td>DSN0603 / SOD962</td>
<td>Single line, ESD protection</td>
</tr>
<tr>
<td>PES2V5Y1BSF</td>
<td>0.25</td>
<td>16</td>
<td>Bidirectional</td>
<td>DSN0603 / SOD962</td>
<td>Single line, ESD protection</td>
</tr>
<tr>
<td>PES3V3Y1BSF</td>
<td>0.26</td>
<td>16</td>
<td>Bidirectional</td>
<td>DSN0603 / SOD962</td>
<td>Single line, ESD protection</td>
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Remark: Single line, ESD protection
New ESD protection products (TrEOS 2)

TrEOS 2 example PESD2V0Y1BSF, VF-TLP 4 kV pulse

Clamping curve

VF-TLP Curve, $T_d = 5\text{ns}$, $\tau_r = 600 \text{ps}$

4 kV clamped down to 16.15 V and 30 V peak, $I_{pp} \sim 78 \text{ A}$
ESD application handbook
Design Engineer’s Guide

• Release of final PDF August 31\textsuperscript{st}

• Available on Nexperia Website:
  • https://efficiencywins.nexperia.com/efficient-products/esd-design-engineers-guide.html

• Print out version available beginning of October
Common mode filters with integrated ESD protection
Common Mode Chokes (1)

**Single-ended Interface**
- Data signal defined via voltage vs ground
- EMI added to the signal line
- Filter concepts are RC and LC low-pass filters

**Differential Interface**
- Data signal defined via differential voltage on a line pair (differential receivers)
- EMI is added to both of the differential signal parts
- Filter concept of the choice are Common Mode filters

Modern high-speed and low-voltage interfaces work in differential mode.
Common Mode Chokes let:

- differential signals pass, but suppress common-mode noise

- Serial data increase data rates
- Reduced line count (less complex connectors, cables and PCB layout)
- Low level differential signals (less radiation and EMC, reliable data transmission)

Common Mode chokes suppress common noise in differential signals
Critical frequencies in combination with USB3.1

USB3.1 @10 Gbit/s fundamental (5 GHz)

For wireless connectivity, portable devices have wireless transmitters, which operate in the same frequency bands as fast data lines, such as USB3.1:

- **GSM 850** – up 824-849 MHz
- **GSM 850** – dwn 869-894 MHz
- **GSM 900** – up 890-915 MHz
- **GSM 900** – dwn 935-960 MHz
- **GSM 1800** – up 1710-1785 MHz
- **GSM 1800** – dwn 1805-1880 MHz
- **GSM 1900** – up 1850-1910 MHz
- **GSM 1900** – dwn 1930-1990 MHz
- **WIFI 2.4** – 2.5 GHz
- **WIFI 4.9** – 5.8 GHz
- **Bluetooth, 2.4-2.5 GHz**
- **GPS/1.2, 1.5 GHz, GLONASS 1.6 GHz**
- **LTE 700/800 MHz, 1700/1900 MHz**
- **LTE 900 MHz, 1.8, 1.9, 2.5, 2.6 GHz**
USB Type-C

- PCMFXUSB3B, differential passband and common mode rejection
USB Type-C

PCMF1USB3B, microscope pictures

WLCSP Packages
5, 10 or 15 balls

For 1, 2 or 3 lanes