Enhance Productivity in PCB Design with Online DFM Checks and Useful FloWare Modules

Holger Schröter
FH Westküste, Heide
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Personal Introduction

Holger Schröter

Studies: Communications Engineering at TU Braunschweig

• Distance control radar at TU Braunschweig
• Development and project management for VCO and frequency synthesizer at Tyco Electronics
• Development of memory modules at Qimonda (Infineon)
• PCB Design Flow und Methodology at Infineon / Intel Mobile Phone
• Application Engineer at FlowCAD
Overview

• DFM (Design for Manufacturing)
  – Taking Manufacturing related requirements into account during design
  – DFM Domains
    • DFF (Design for Fabrication): Checks related to plain PCB Manufacturing
    • DFA (Design for Assembly): Checks related to Component Mounting
    • DFT (Design for Testing): Checks related to Testing

• FloWare
  – Digital Soldermask
  – Edge Plating
DFM – Design for Manufacturing
Design for Manufacturing

- Design for Fabrication
  - Min Shape Width
  - Annular Rings
  - Mask Slivers
  - Mask Island

- Design for Assembly
  - Package Spacing
  - Mechanical Hole to Component

- Design for Test
  - Testpoint to Testpoint Spacing
  - Testpoint to Component Spacing
DFM Examples

• Typical examples for manufacturing issues, which can easily be avoided during design
  – Zollner Elektronik AG
  – AT&S
  – Würth Elektronik
  – Cadence
  – Nvidia
DFM Examples Zollner (I)

DFM: Issue solder balls

DFM analysis of C283 (C282, C279)

Both toeprints of the component are not placed on an equal sized pad. The pads are too big for the toeprints.

Source: Zollner Elektronik AG

Reality on board

This can cause solder balls under the component!
DFM Examples Zollner (II)

DFM: Trace under component

- Lines under zero, stand-off components (such as discrete or resistor pack components, lying close to the board) can interfere with proper placement. Tombstoning or a stand-off can be possible.

Source: Zollner Elektronik AG
DFM Examples Zollner (III)

DFM: Hole in SMD Pads

• Reports of holes in SMD pads. Please avoid holes in SMD pads. If there are any, they must be plugged otherwise they should be removed

• For example here in a heatsink landpattern

• If the holes / vias are treated in a proper style it would be no issue any more
• Please care about the IPC-4761 type VII (filled and capped)

Source: Zollner Elektronik AG
DFM Examples AT&S (I)

Optimal pad / soldermask 1:1

Increased soldermask remaining path too small

Increased soldermask, no more gap between soldermask pads available

Source: AT&S
DFM Examples AT&S (II)

Source: AT&S
DFM Examples AT&S (V)

Pseudo Errors During AOI

- Rework on pad connections between pads on the same net
  - Usually areas with more than 200 pads per layer

- Areas marks in white represent the pseudo errors during AOI
  - Highlighted areas have ≤50μm spacing, which is critical during etching process
  - Result: Possible undefined shorts between pads on multiple layers (+200 errors per layer during AOI)

- Additional steps for CAM
  - During preparation, CAM team has to connect each pad individually
  - This rework process and net list modification can take hours for CAM team to complete

Note: Please check the design (modify if needed) to prevent these errors from occurring!

Source: AT&S
DFM Examples AT&S (VI)

- Restring requirement for PTH / Via (125 µ circulating)
- Depending the production process
- Annular Ring Check in DFF
DFM Examples AT&S (VII)

- Copper filled µVia
- Unfilled µVia
- Unfilled Via
- Filled Via
- Staggered µVias
- Built-up
- Stacked µVias at same position
- Through hole and µVias at same position

Source: AT&S
DFM Examples Würth Elektronik (I)

• Hull break due to adverse aspect ratio
  – Different thermal expansion of FR-4 and copper

• Aspect ratio check in DFF

Source: Würth Elektronik
DFM Examples Würth Elektronik (II)

- Aspect Ratio Check
DFM Examples Würth Elektronik (III)

• Solution: Laser drilled microvias
  – Short hulls are not likely to break

Source: Würth Elektronik
DFF Examples Cadence (I)

- Outline / cutout spacing
  - Trace too close to a cut-out

- Silkscreen
  - Silkscreen to silkscreen
  - Silkscreen to pad

Source: Cadence
DFF Examples Cadence (II)

- Copper feature
  - Acid trap in a shape

- Soldermask
  - Solder paste wicking
  - Maximum exposed etch in soldermask

Source: Cadence
GeForce RTX 3000: Stability Problem (I)

- Stability problem due to capacitors under graphic chip

Source: www.heise.de
GeForce RTX 3000: Stability Problem (II)

- Might be a design / manufacturing issue
  - Pad design
    - Copper
    - Soldermask
    - Pastmask
  - Vias in pads
  - Solder process

Source: www.heise.de
Earlier is Cheaper

- Late discovered errors get more expensive
  - Iterations
  - Prototypes
  - Redesigns
  - Missed market entry

- Avoiding errors by early detection saves costs
  - Signal- and Power-Integrity
  - Manufacturing, Assembly and Test
    - DFM, DFA, DFT, …
  - Thermal
  - EOL

Cost of different timing:
- Alternate circuit idea: 1 €
- Changes in schematic: 10 €
- Changes in PCB Layout: 100 €
- Changes after CAM / DFM check: 1,000 €
- Redesign after prototype: 10,000 €
- EOL-Redesign after market introduction: 100,000 €
- World wide recall due to malfunction: 1,000,000 €
Traditional PCB Design Flow

• DFM Checks are done after design is finished
• Time-consuming design cycles in case of manufacturing issues
• Design loops required to guarantee manufacturability
In-design DFM Checks Flow

- First time right
  - By using production proved DFM rules from manufacturing
  - By online DFM rules check during design

- Manufacturing related checks are online during PCB Design
  - No re-spins required
DesignTrue DFM Ecosystem

• On-line Rule Description
  – Describes rule intent

• Inherited Values
  – Major categories populate children of rule
  – Allows independent rule entry definition

• Download completed sets
  – Uses web tool download location
  – No data stored on server, download to client
DFM Portal

- Cadence offers DFM Portal to request DFM rules at PCB Manufacturer
  - Production proven rules
  - No need to enter manually
Web-based Rules Request

• PCB Designer can request rules sets in web portal
  – https://pcb.cadence.com/dfm_customer
Web-based Rules Description

- Manufacturer can enter rules in web portal
  - https://pcb.cadence.com/dfm_vendor
DFM Wizard

• Automated import of rules sets
• Wizard guides through import process
• Automated adaption to stackup and technology
DFF and DFA Checks

• DFF Constraints
  – Outline (cutout)
  – Mask
  – Annular ring
  – Copper spacing
  – Silkscreen

• DFA Constraints
  – Outline
  – Spacing
  – Pastemask
  – Fiducial
# Fabrication DRC Examples (DFF)

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Usage</th>
<th>Picture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mask Sliver</td>
<td>This specifies the minimum width of a mask where the potential for mask material deposited may become delaminated from the PCB substrate. Checks are based on the mask layer being the standard negative image use model</td>
<td>Non-Etch</td>
<td><img src="image" alt="Mask Sliver" /></td>
</tr>
<tr>
<td>Mask Islands</td>
<td>This specifies the minimum square area of mask material, where if the mask area is too small, may delaminate from the PCB. Checks are based on the mask layer being the standard negative image use model</td>
<td>Non-Etch</td>
<td><img src="image" alt="Mask Islands" /></td>
</tr>
<tr>
<td>Pin Hole to Pad</td>
<td>The minimum distance of the pin padstack hole to the outermost edge of the pad geometry</td>
<td>Etch</td>
<td><img src="image" alt="Pin Hole to Pad" /></td>
</tr>
<tr>
<td>Outline to Pin Pad</td>
<td>The clearance between any Pin pad edges to the DESIGN_OUTLINE geometry</td>
<td>Etch, Non-Etch</td>
<td><img src="image" alt="Outline to Pin Pad" /></td>
</tr>
<tr>
<td>All Pin Pads</td>
<td>This specifies the minimum allowable distance of any silkscreen geometry to the edge of a pin pad</td>
<td>Non-Etch</td>
<td><img src="image" alt="All Pin Pads" /></td>
</tr>
</tbody>
</table>

Total Number of DFM Rules: ~ 2.500
# Assembly DRC Examples (DFA)

<table>
<thead>
<tr>
<th>Rule</th>
<th>Description</th>
<th>Usage</th>
<th>Picture</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pastemask to Outline</td>
<td>Checks the space between the DESIGN_OUTLINE geometry and the edge of any PASTEMASK geometry. Any measured value smaller than the rule value is reported as a DRC. Paste mask layers must be defined in the design Cross-section</td>
<td>Non-Etch</td>
<td><img src="image" alt="Pastemask to Outline" /></td>
</tr>
<tr>
<td>Component body to tooling hole</td>
<td>Defines the minimum allowable distance between edge of a component instance to a tooling hole</td>
<td>Etch</td>
<td><img src="image" alt="Component body to tooling hole" /></td>
</tr>
<tr>
<td>Pastemask to Pad</td>
<td>Checks the space between the edge of any PASTEMASK geometry and to component's SMD pin pad</td>
<td>Non-Etch</td>
<td><img src="image" alt="Pastemask to Pad" /></td>
</tr>
<tr>
<td>Trace under Component</td>
<td>Defines the list of package symbols where traces are not permitted under the component boundary</td>
<td>Etch</td>
<td><img src="image" alt="Trace under Component" /></td>
</tr>
<tr>
<td>Large Via under component</td>
<td>A Yes value displays a DRC for any large vias under any component body. A No value turns the check off for this rule</td>
<td>Etch</td>
<td><img src="image" alt="Large Via under component" /></td>
</tr>
</tbody>
</table>

Total Number of DFM Rules: ~ 2.500
FloWare
FloWare Features

• General purpose utilities
  – Functions not in standard tool yet
  – Not written for one specific customer
  – Everybody should benefit

• Easy installation
  – Also casual users must be able to install FloWare
  – No variables
  – Menus will be created automatically
  – Integrates perfectly into existing customizations

• Documentation
  – Full documentation is provided for every module
FloWare Modules Overview

• Advanced Mirror
• Advanced Testpoint Check
• Anti Tamper Mesh PCB
• AOI Check
• Assign Net to Via
• Barcode Generator
• Batchplot
• CAF-DRC
• Change Width
• Class Color
• Cleanliness Check
• Coil Designer
• Contour Place
• Cross Copy
• Cross Section Generator
• Custom Variables
• Design Compare
• **Digital Soldermask**
  • Drafting Utilities
  • Drawing Designer
  • Drawing Size
  • Drawing View Manager
• **Edge Plating**
  • FPGA Utilities
  • Highlight Dummy Pins
  • IBIS Prototype Modeler
  • Label Generator
  • Label Tune
  • Mask Generator
  • NC Panel Route
  • Net Color View
  • Padstack Finder
  • Padstack Usage
  • Panelization
  • PCB Library Plot
  • Polar Grid Utilities
  • Post Processing
• Push to Grid
• Quick Symbol Edit
• Replace Via
• Shape Utilities
• Shield Generator
• Shield Routing
• Silkscreen
• Snap Generator
• SVG Export
• Synchronize Testprep
• Variant 3D
• Variant Assembly
• Variant BOM
• Z-DRC
Digital Soldermask

Pad box

Trace mode

Component boundary

Soldermask region
Digital Soldermask

- Developed together with Würth Elektronik
- Various modes
  - Pad ring / box
  - Trace mode
  - Component mode
  - By region
- Parameters
  - Bridge width
  - Pin, via gap
  - Length offset
  - …
Digital Soldermask

- Techniques can be combined and used to create multiple masks on separate layers, accounting for mask thickness requirements

In example above:
- Soldermask region on Digital_Soldermask_1_TOP
- Pad box on Digital_Soldermask_2_TOP
- Pad box on Digital_Soldermask_3_TOP

2D

3D canvas
Edge Plating

• Edge plating is a plated conductive material on the edge of a PCB where in normal instances, only dielectric material is exposed

• This plated conductive material may be used for many functions
  – Improve current carrying across multiple layer of a PCB
  – Edge connection protection
  – Board to case grounding
  – EMC signal integrity
  – Heat management

• Two forms of Edge Plating
  – Wraparound (Side) Plating
  – Castellated Holes
Edge Plating: Wraparound (Side)

- Define plating sections interactively
- Net assignment
- Connectivity Check
- DRC Clearance Check
- Net Short support
Edge Plating: Castellated Holes

- Define locations interactively along outline supporting
  - Spacing
  - Quantity

- Objects supported
  - Vias
  - Via structures
  - Symbols
  - Electrical components

- Placement parameters
  - Alignment with outline (relative, absolute)
  - Offset from outline
FloWare Link Tips

- Overview of All Available FloWare Modules
- Free Trial
- FloWare Datasheet
- FloWare Detailed Description
- Videos @ YouTube
Products / Solutions for Electronic Designers

Solutions
• PCB Layout
• PSpice-Simulation
• SI- and PI-Simulation
• EMI and Antenna Simulation
• Timing Analysis
• Thermal Simulation
• 3D mCAD-eCAD Integration
• CAM Verification
• Boundary Scan Test
• Protocol Analysis
• Electronic Data Management
• PLM and ERP-Connection
Focus on Customer Satisfaction

Sales
• Fair, competent advice
• Long term solutions

Support
• Hotline, Fastviewer
• Survey

Service
• PCB Design Services (Layout, Simulation, Migration)

Training
• Trainings center, on-site
• Workshops
Contact us / Kontakt zu FlowCAD

Please do not hesitate to contact us.
Für weitere Fragen und Informationen stehen wir gerne zur Verfügung.

FlowCAD Deutschland
Mozartstr. 2
85622 Feldkirchen bei München
T +49 89 45637-770
info@FlowCAD.de

FlowCAD Schweiz
Hintermättlistr. 1
5506 Mägenwil
T +41 56 485 91 91
info@FlowCAD.ch

FlowCAD Polska
ul. Sąsiedzka 2A
80-298 Gdańsk
T +48 58 727 90 90
info@FlowCAD.pl
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